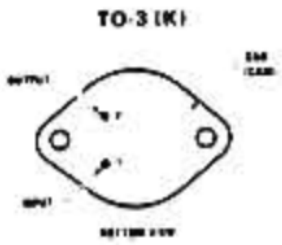
Eventide
the next step

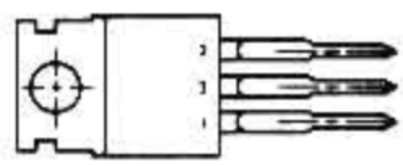
digital delay lines
instant flangers
omnipressors
harmonizers
monstermats

EVENTIDE CLOCKWORKS, INC • 265 WEST 54TH STREET• NEW YORK, N.Y 10019 • 212-581-9290

LM323 - 3 amp, 5 volt positive regulator



7812UC - 12 volt regulator
7815UC - 15 volt regulator
7915UC - minus 15 volt regulator



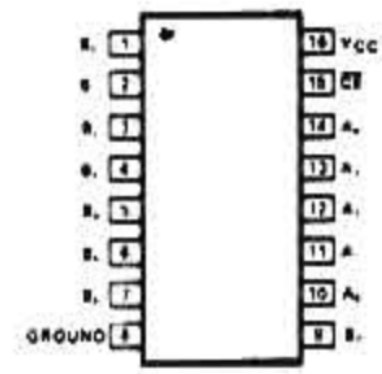
	7812UC + 7815UC	7915UC
	output	output
	common	input
	input	common

82S123 or 74S288 - 256 Bipolar PROM (32 x 8)

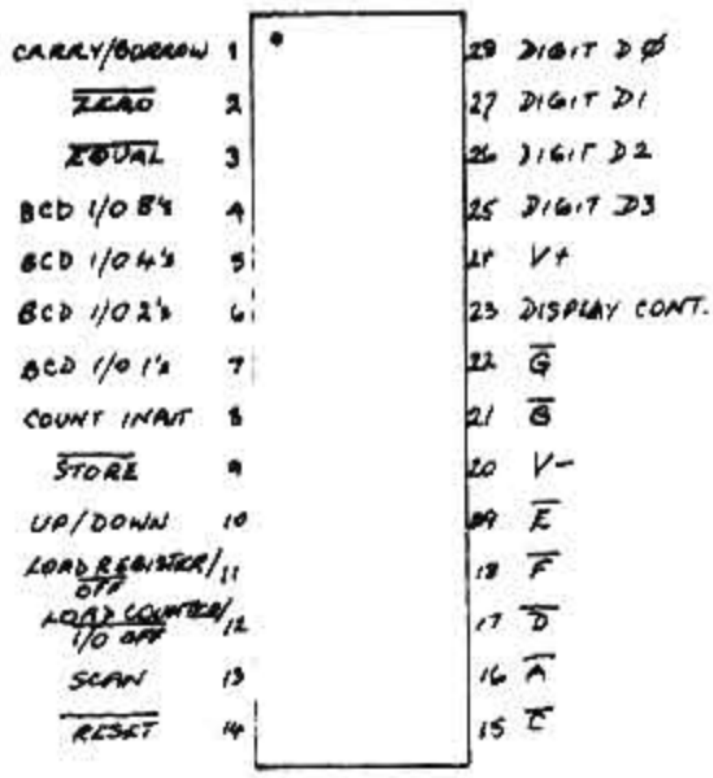
VERY IMPORTANT NOTE:

All parts with the above marking are FACTORY PROGRAMMED, and will fit only into their own specific locations on each circuit board. THEY ARE NOT INTER-CHANGEABLE. For example, you cannot exchange IC60 and IC61 on the HD921 board - they have been programmed differently, and their characteristics are completely different.

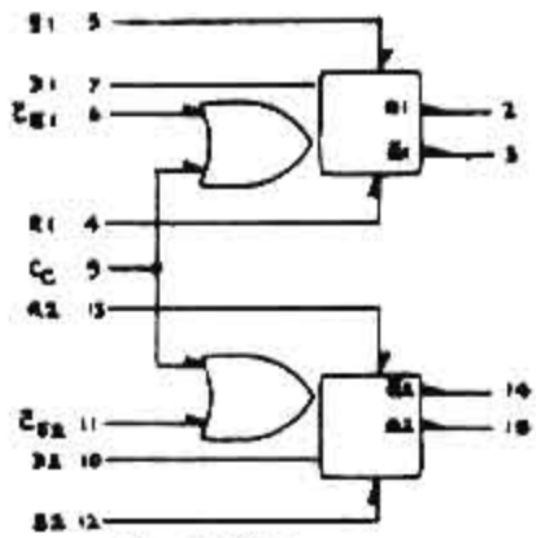
Should you ever need replacements for any of these parts, you must specify the board number and the IC number, to ensure receiving the correct replacement.



ICM7217 - Complementary MOS 4-digit Up/Down counter-decoder-driver



MC10131 Dual D-Type Master/Slave Flip-Flop



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

CLOCKED TRUTH TABLE

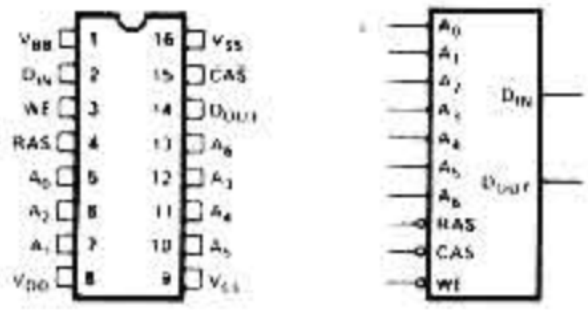
C	D	Q_{n+1}
L	Ø	Q_n
H	L	L
H	H	H

Ø = Don't care
C = $\overline{C_E} + C_C$
A clock H is a clock transition from a low to a high state.

APPENDIX Integrated Circuits used in the H949 Harmonizer

16 K Dynamic RAM (various manufacturers and part numbers)

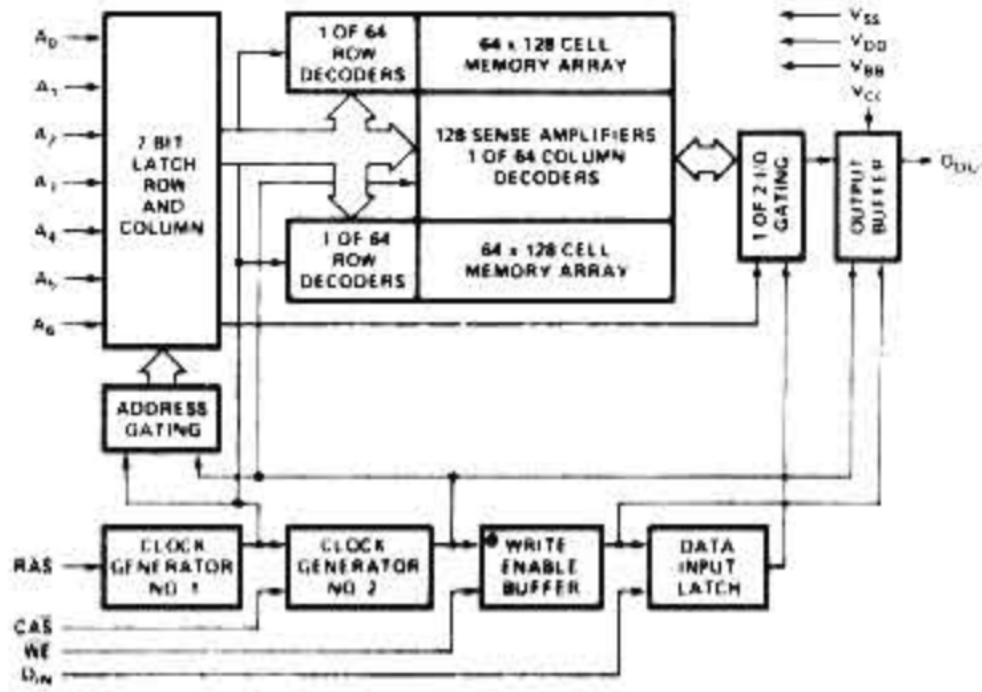
PIN CONFIGURATION **LOGIC SYMBOL**



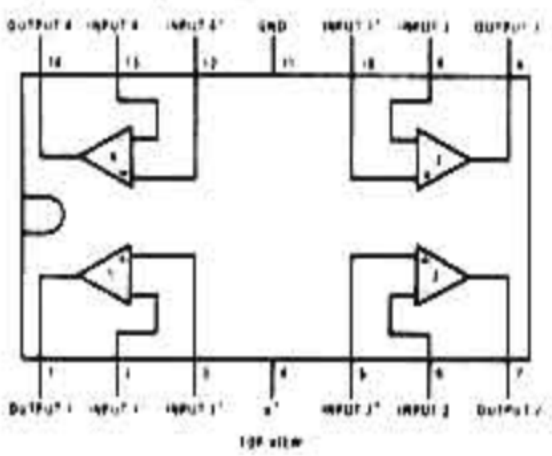
PIN NAMES

A_0-A_6	ADDRESS INPUTS	WE	WRITE ENABLE
CAS	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
RAS	ROW ADDRESS STROBE	V_{SS}	GROUND

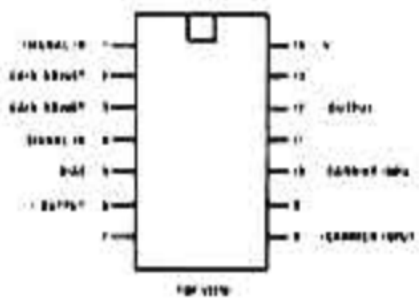
BLOCK DIAGRAM



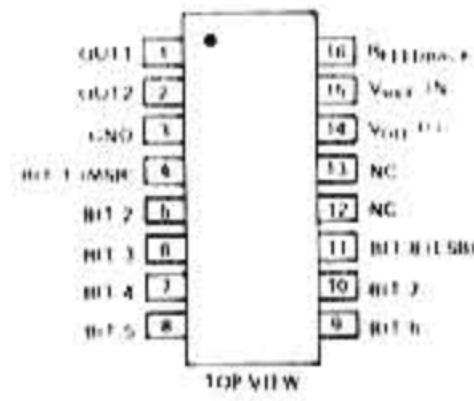
TL064
Quad op amp



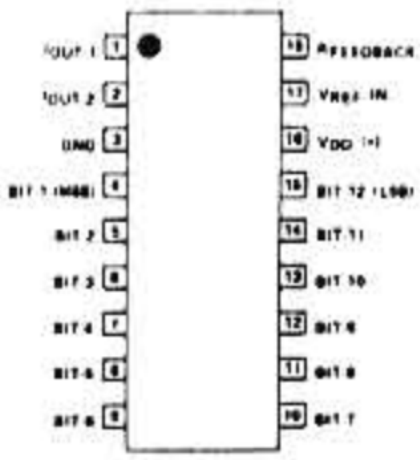
LM1496
Balanced modulator-demodulator



AD7523
8 Bit D/A converter



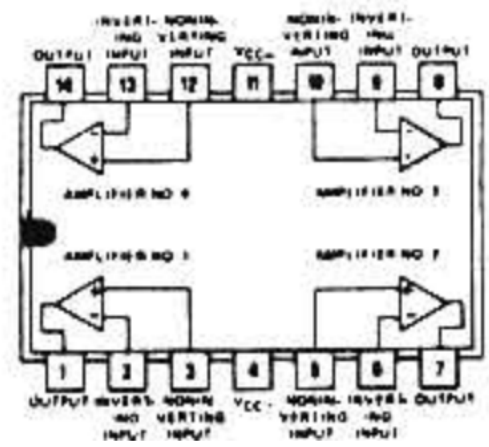
AD7531 - 4-Quadrant Multiplying D/A Converter



AM2901 - Four-bit bipolar micro-processor slice

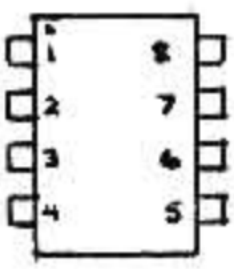
TL081 - JFET-Input Operational Amplifier

TL084 - JFET-Input Quad Operational Amplifier



RC4151 - Voltage to Frequency Converter

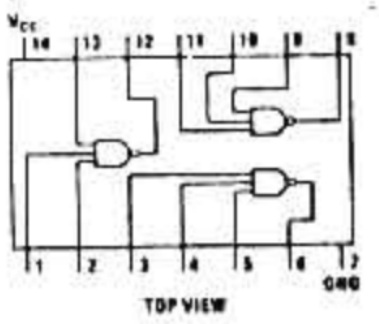
current source
scale factor
logic output
ground



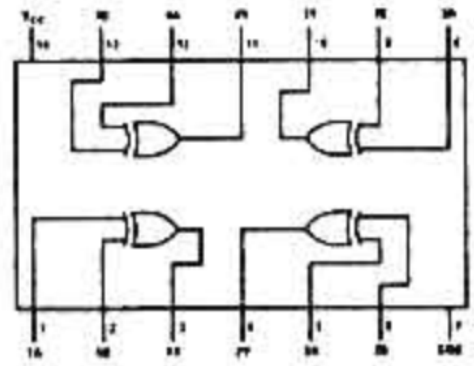
V_{CC}
input voltage
threshold
one shot R,C

APPENDIX Integrated Circuits used in the H949 Harmonizer

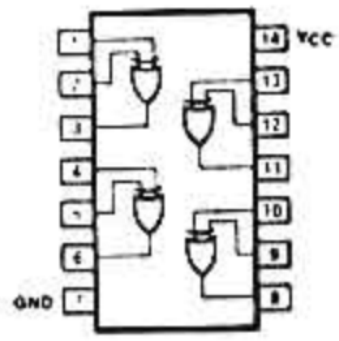
74C10
Triple 3-input
NAND gate



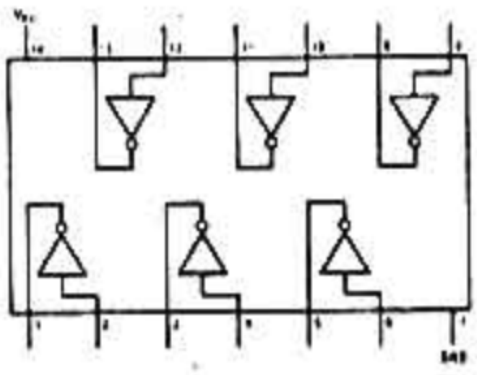
74C86
Quad 2-input
Exclusive-OR gate



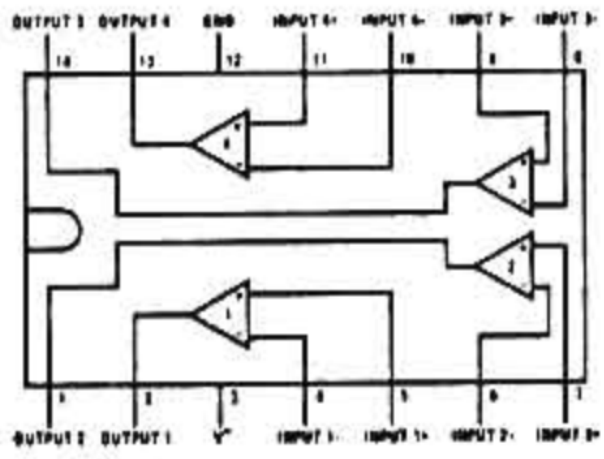
74LS86
Quad 2-input
Exclusive-OR gate



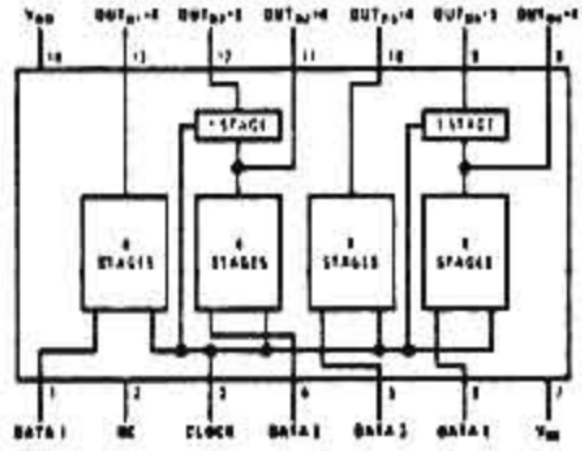
74C901
Hex inverting
TTL buffer



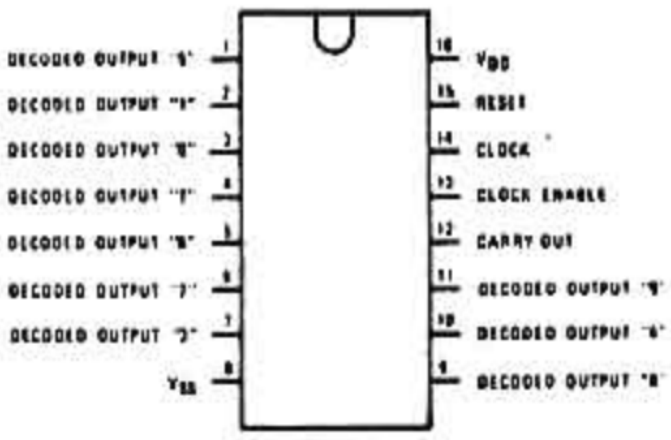
74C909
Quad comparator



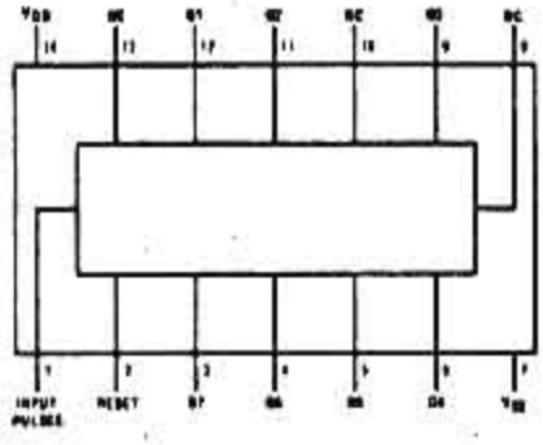
CD4006
18-stage static
shift register



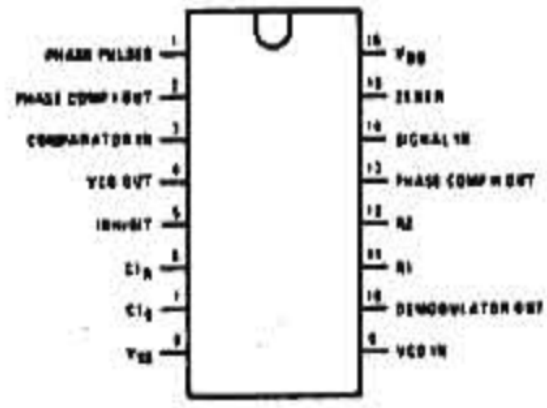
CD4017
Decade counter/divider with
10 decoded outputs



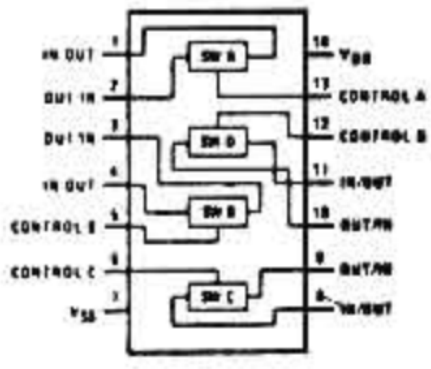
CD4024
7-stage ripple-carry
binary counter/divider



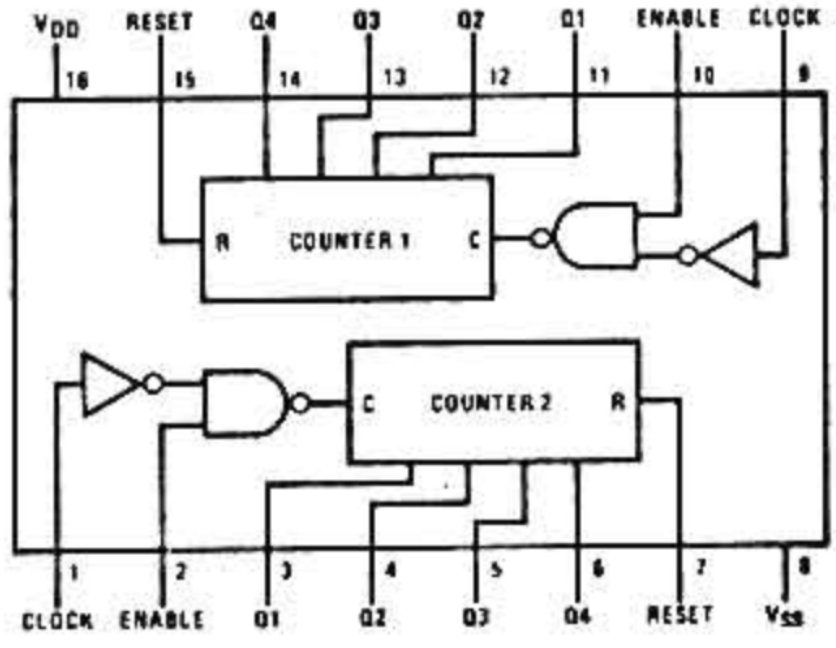
CD4046
Micropower
phase-locked loop



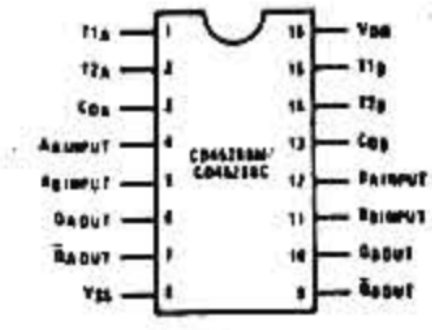
CD4066
Quad bilateral switch



CD4518, MC14518
Dual synchronous up counter

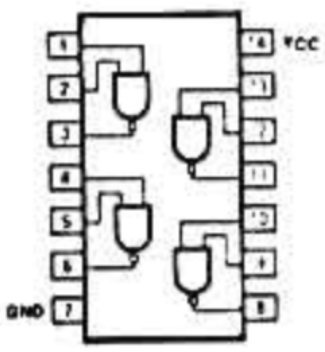


CD4528, MC14528
Dual monostable
multivibrator

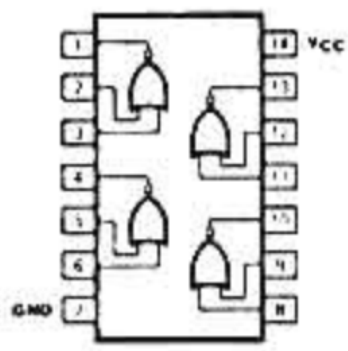


APPENDIX Integrated circuits used in H949 Harmonizer

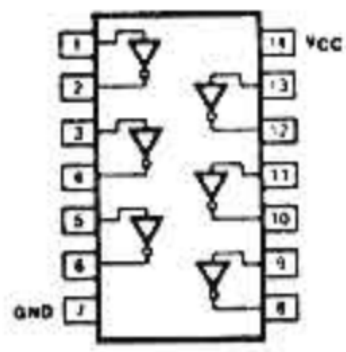
74LS00, 74C00
Quad 2-input
NAND gate



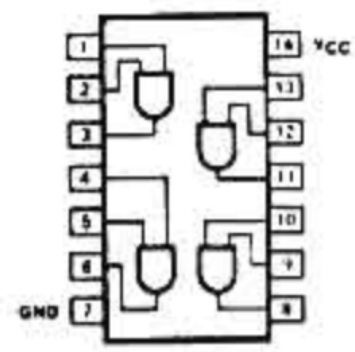
74LS02, 74C02
Quad 2-input
NOR gate



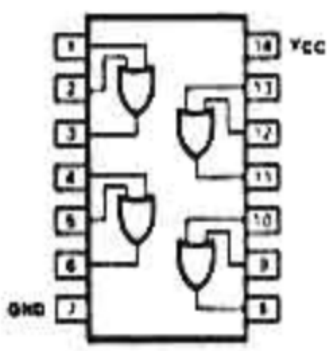
74LS04, 74C04
Hex inverter



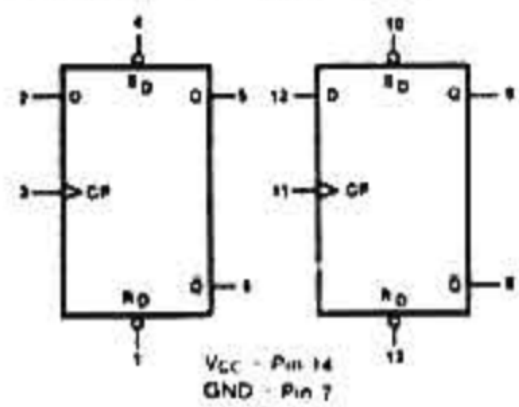
74LS08, 74C08
Quad 2-input
AND gate



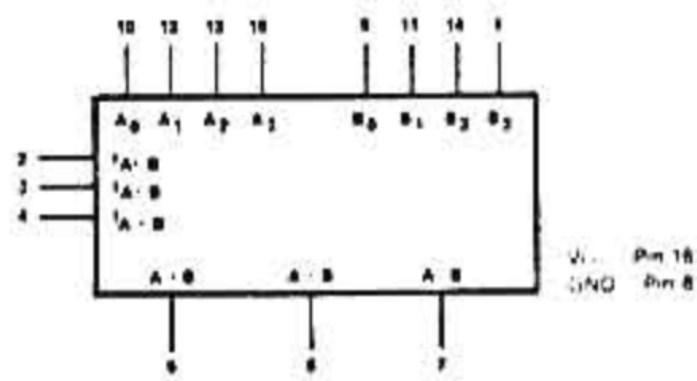
74LS32
Quad 2-input
OR gate



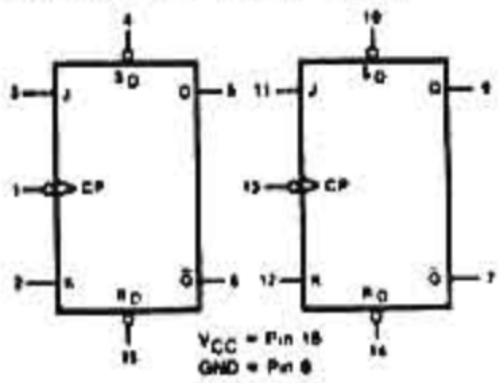
74LS74, 74C74
Dual positive edge-
triggered flip-flop



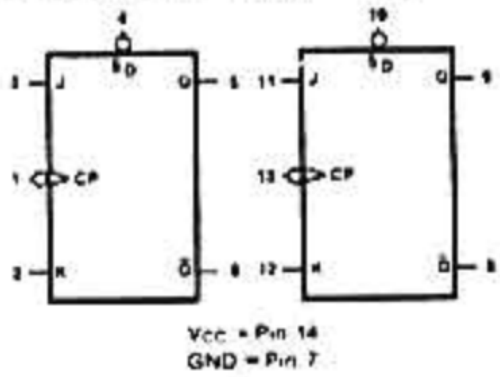
74LS85
4-bit magnitude
comparator



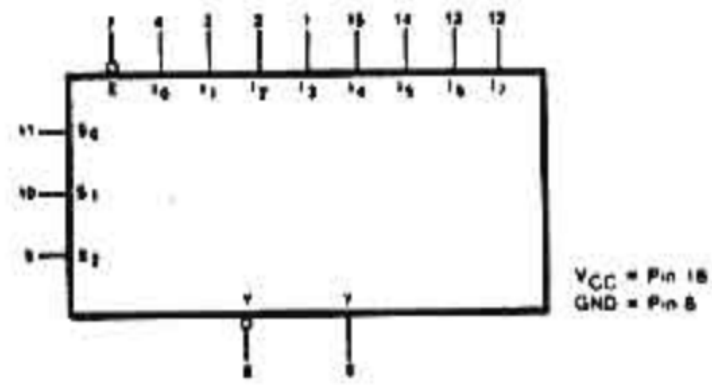
74LS112, 74S112
Dual JK negative edge-
triggered flip-flop



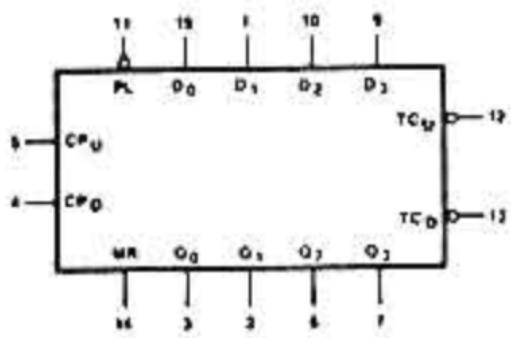
74LS113, 74S113
Dual JK negative edge-
triggered flip-flop



74LS151
8-to-1 multiplexer

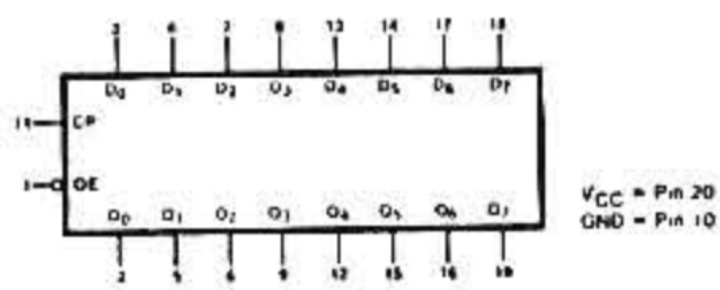


74LS192
BCD decade
up/down counter

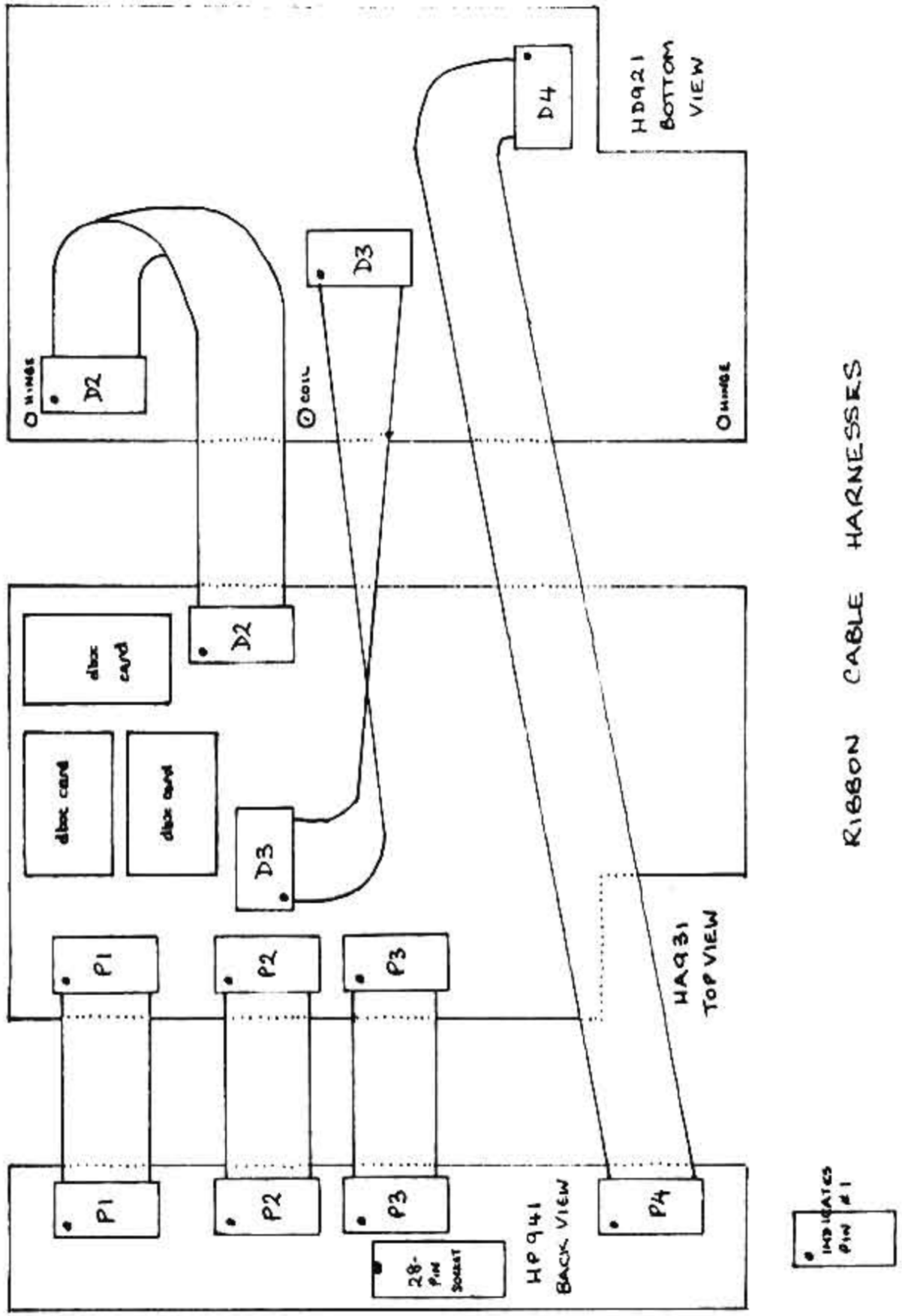


74LS193, 74C193
4-bit binary
up/down counter

74LS374
Octal D flip-flop (3-state)



APPENDIX - Ribbon Cable Harnesses used in H949 Harmonizer



RIBBON CABLE HARNESSES

HA 931 — HP 941

P1

EQOUT	8	7
DLYFB		
		+15v
-15 v		GROUND
LEVEL OUT		GROUND
LEVEL IN	14	1

P2

DLY	8	7
FPR		
RMCV		
+12v		
LMT		
PRS		
+5v	14	1

GROUND	
CNT	
RPT	
NRM3	
NRM2	
NRM1	

P3

$\overline{RND}$	8	7
$\overline{FLG}$		
$\overline{\mu PC1}$		
$\overline{\mu PC\#}$		
$\overline{REVS}$		
$\overline{EXT}$		
$\overline{NPC}$	14	1

ALG1
RMPR
SREFA
SREFB
MANV
CV+M
KYBD

HD921 — HA931

D1

+12v
GROUND
+5v
+5v
GROUND
+12v

D2

RPT	8	7
$\overline{RSTFIFO}$		
FLNG		
PNTR		
GROUND		
+15 v		
MDAC	14	1

RDFIFO
DLAY
CMP
SAMP
GROUND
DDAC
-15v

D3

GROUND	8	7
AD6		
AD7		
AD8		
AD9		
AD10		
SREFB	14	1

SREFA
PC2
NWRT
$\overline{REV}$
ALG1
$\overline{RVF}$
EXTD

HD921-HP941

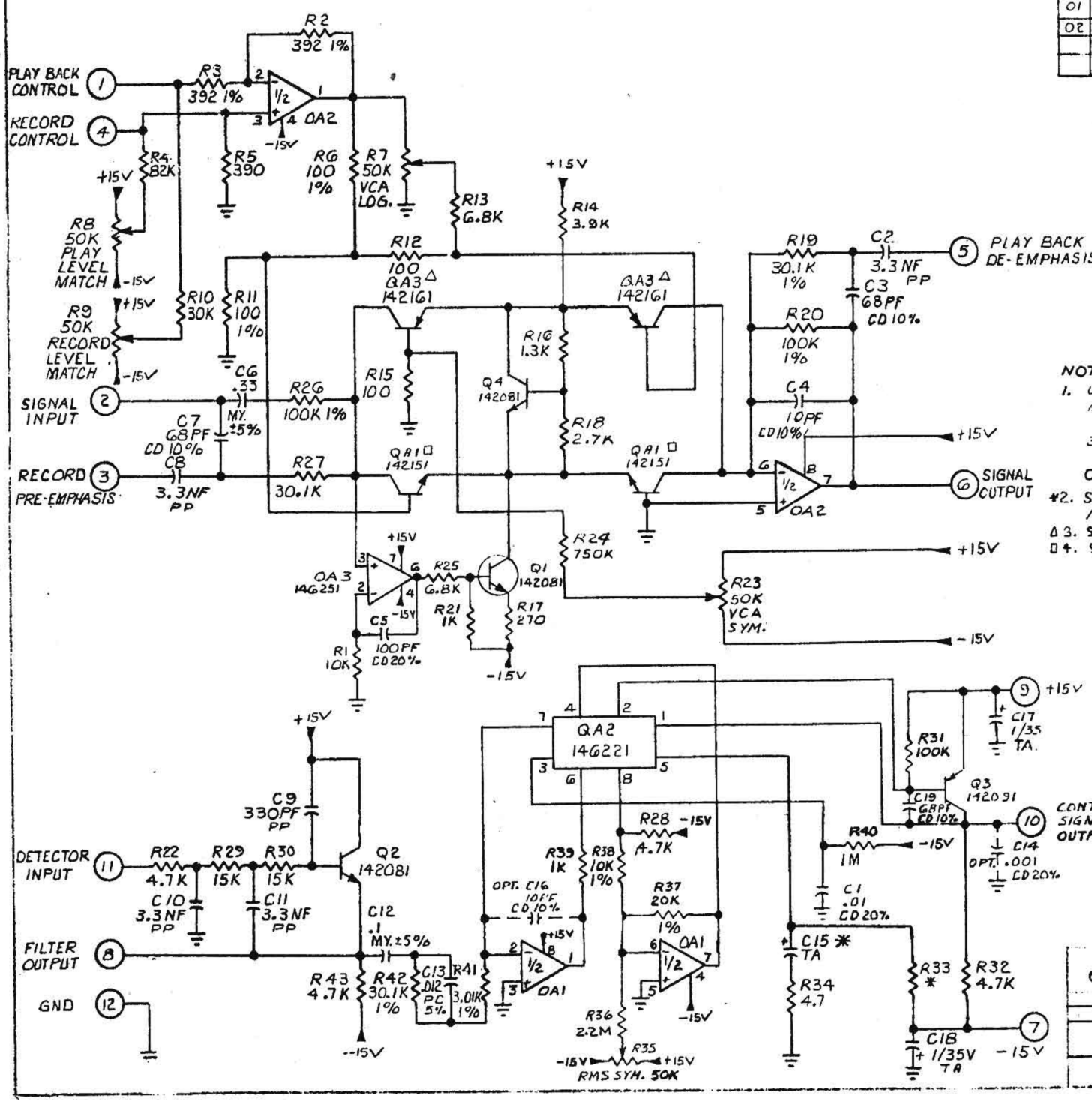
D4

D8	8	7
D9		
D10		
D11		
D12		
D13		
D14	14	1

D7
D6
D5
D4
D3
D2
D1

INTER-BOARD CONNECTORS

REV	DESCRIPTION		DATE
01	PER ECO#435	PT	8-21-78
02	PER ECO# 450	DT PT	11-10-78



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE EXPRESSED IN OHMS AND ARE VAW ± 5%.
   B. CAPACITORS ARE EXPRESSED IN MICROFARADS.
   C. OP AMPS ARE #146241.

#2. SELECT C15 + R33 PER SPEC. DWG. A164001.

△3. SELECT QA3 PER. SPEC. DWG. 160002.

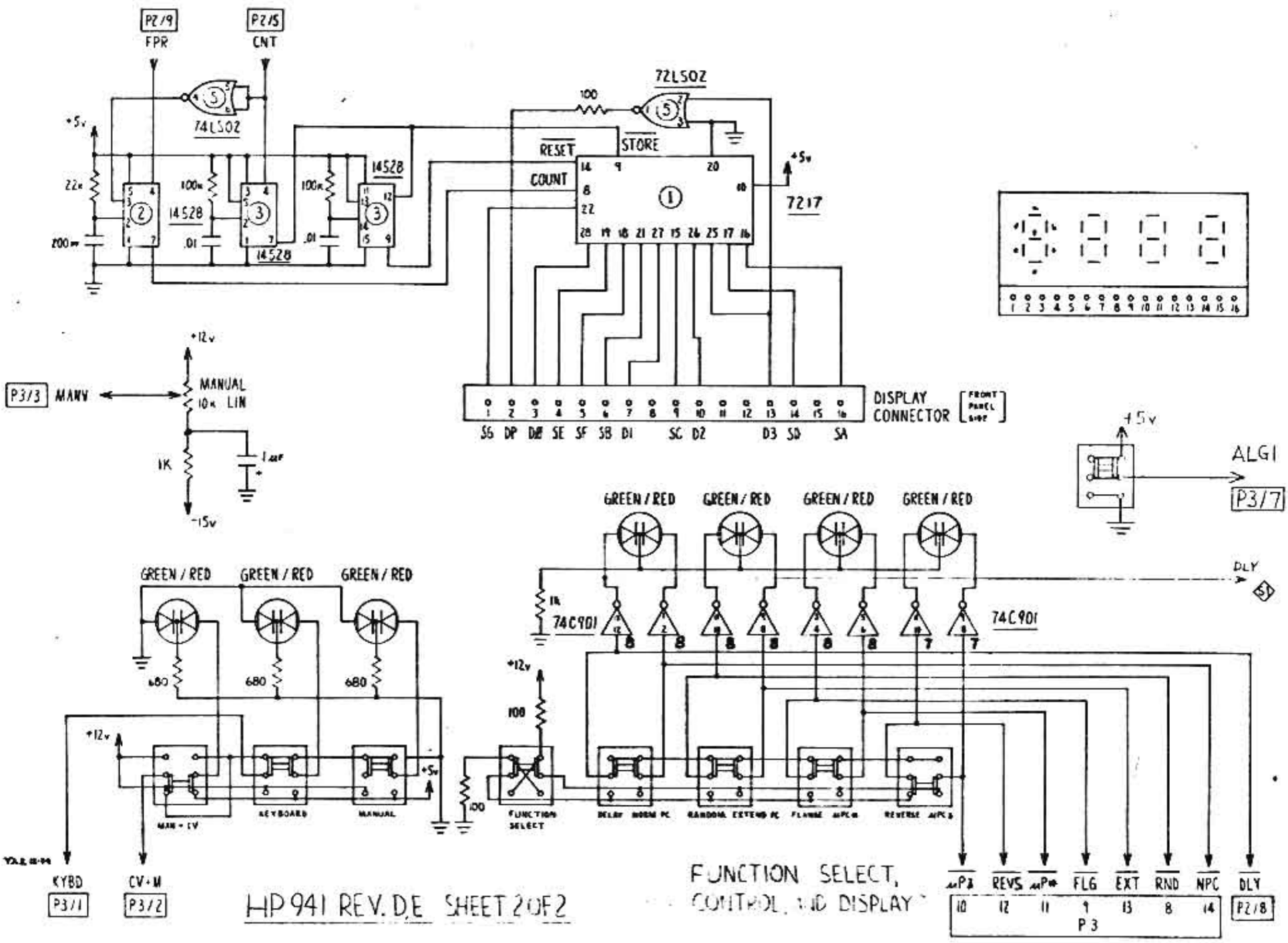
□4. SELECT QA1 PER. SPEC. DWG. 160016.

dbx inc. WALTHAM, MASS.

	JFC 29 JAN 79		
4/11/79	RELEASED BY:	CHKD BY: PT	

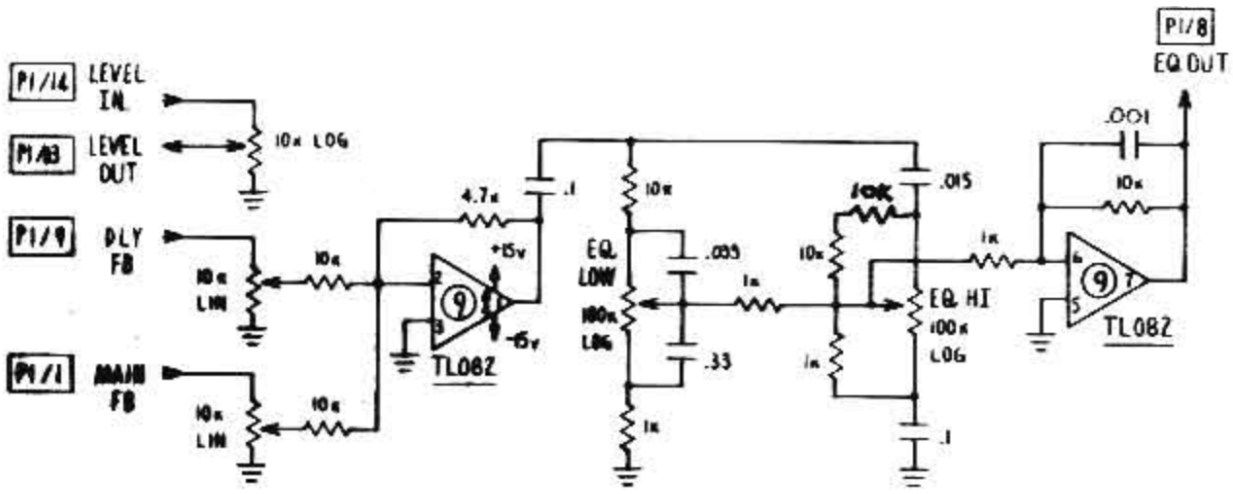
SCHEMATIC
MODEL 303C TYPE II 15V

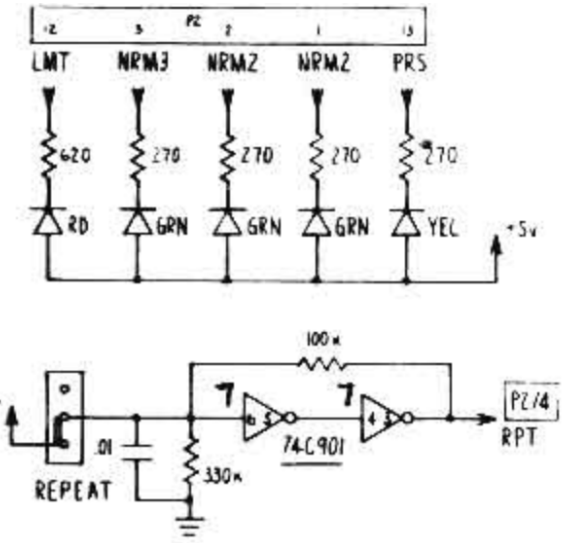
340123 02

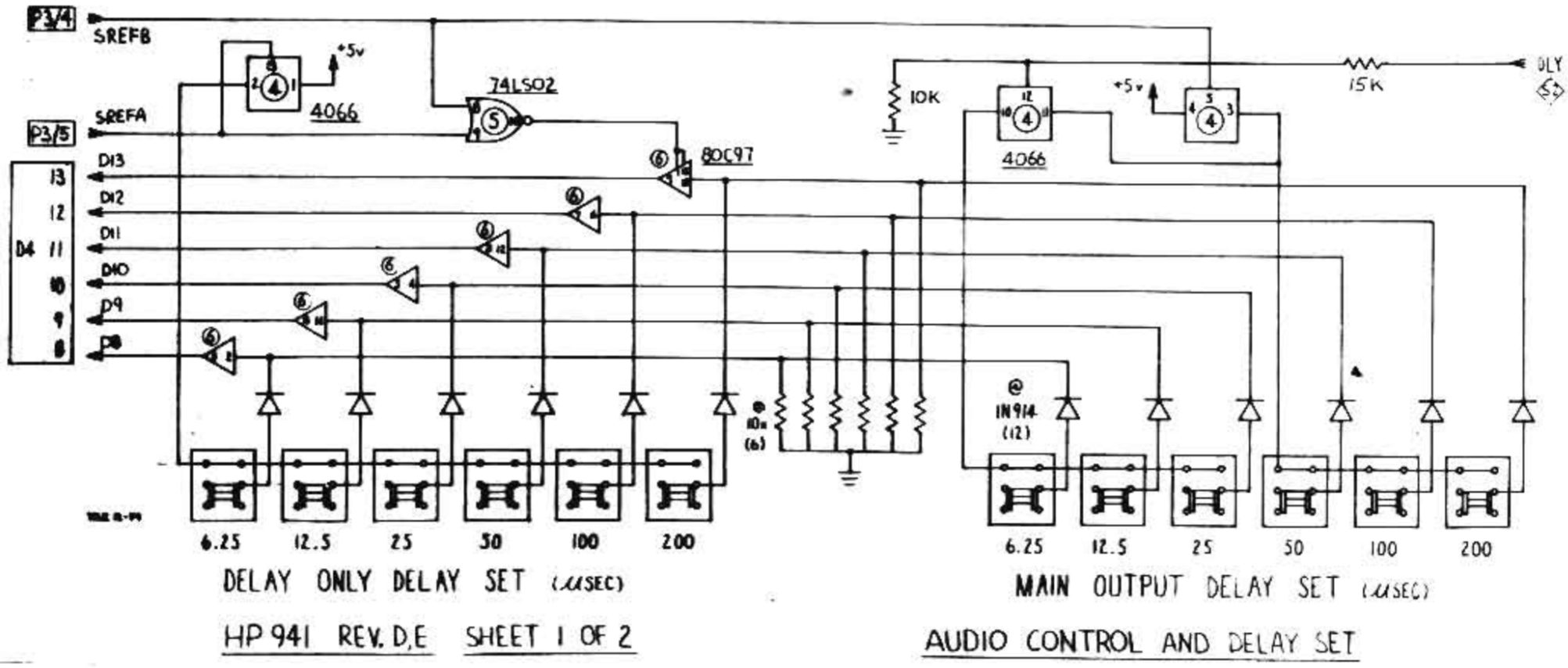


HP 941 REV. D,E SHEET 2 OF 2

FUNCTION SELECT, CONTROL AND DISPLAY

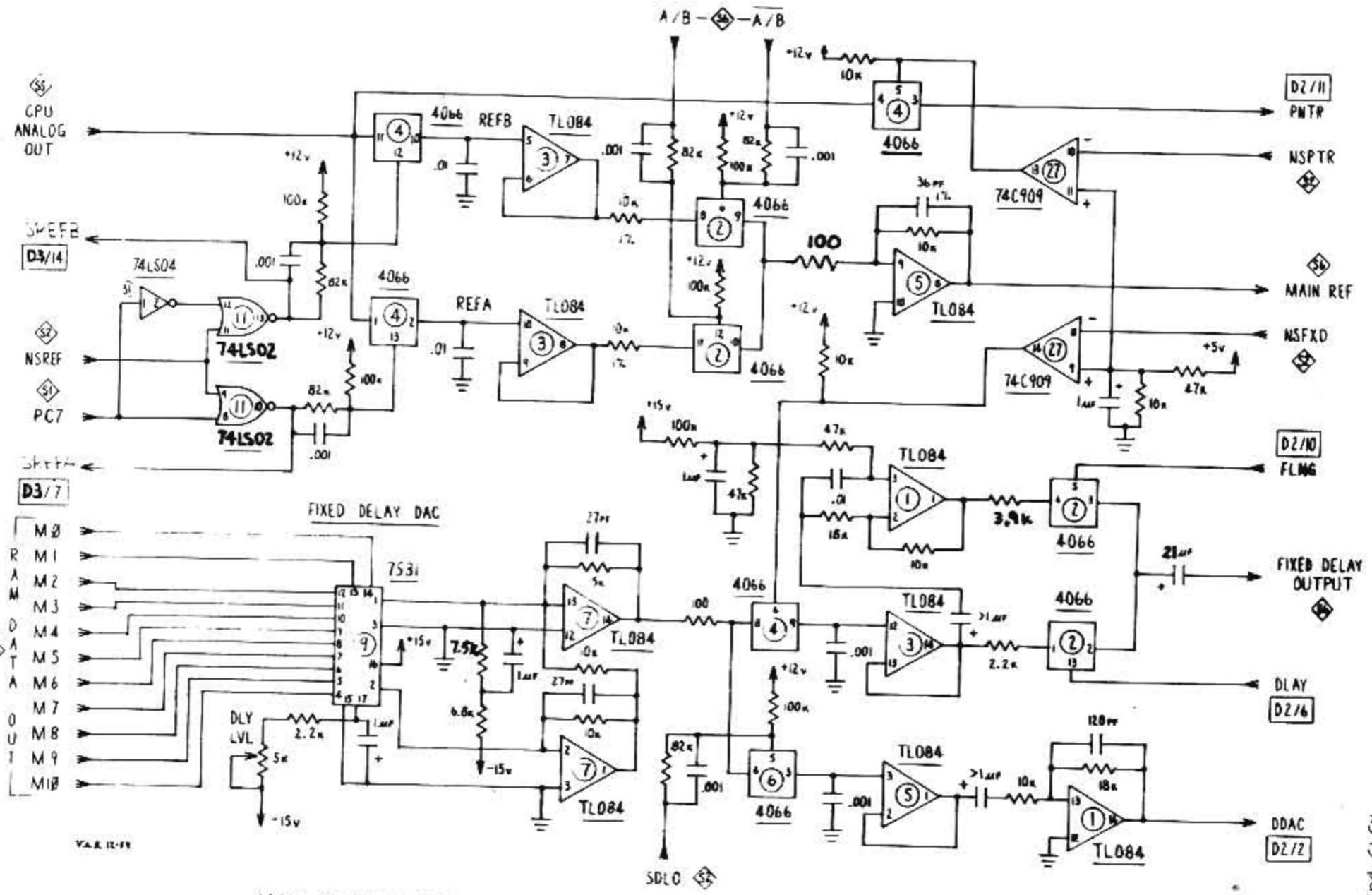






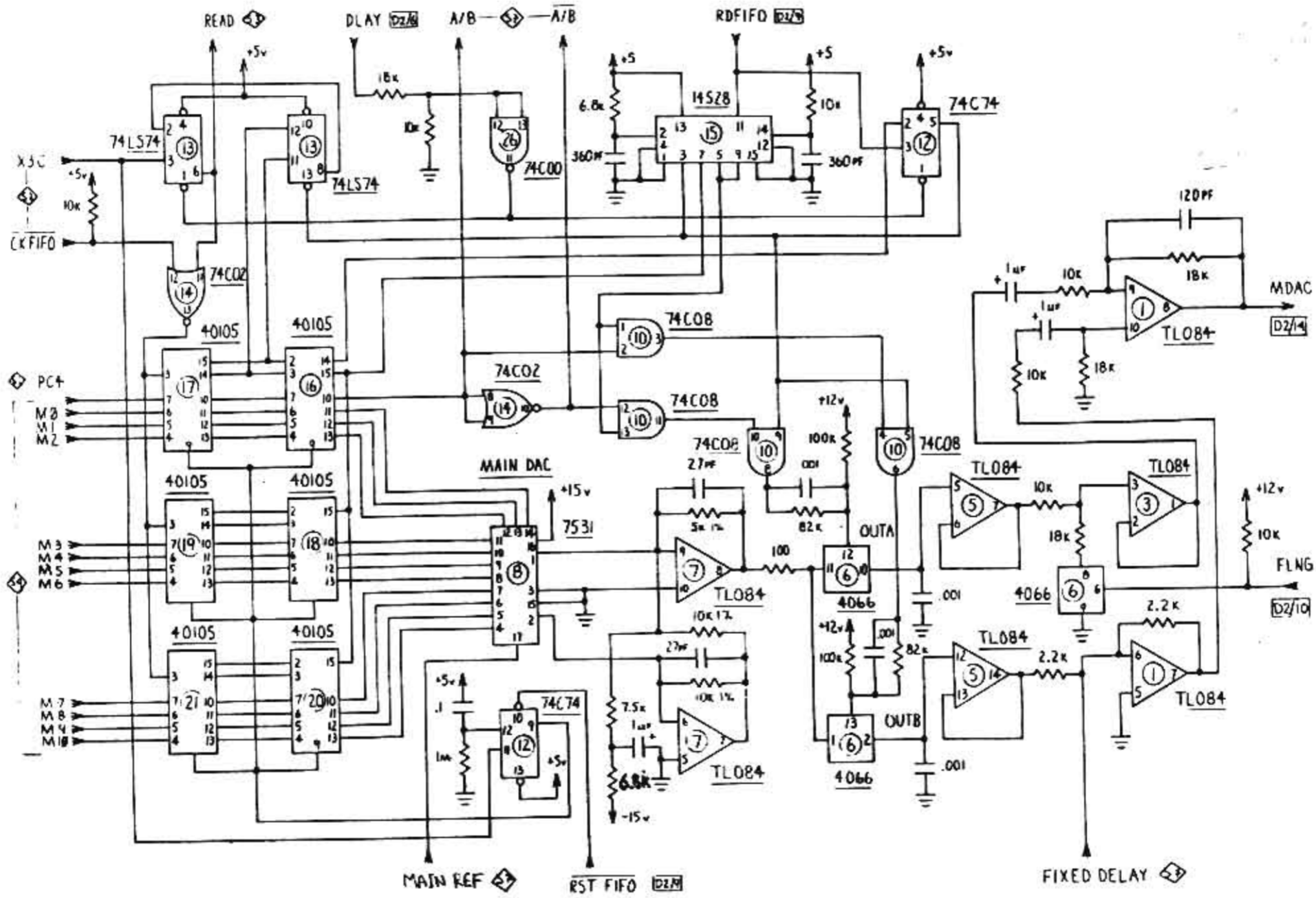
HP 941 REV. D,E SHEET 1 OF 2

AUDIO CONTROL AND DELAY SET



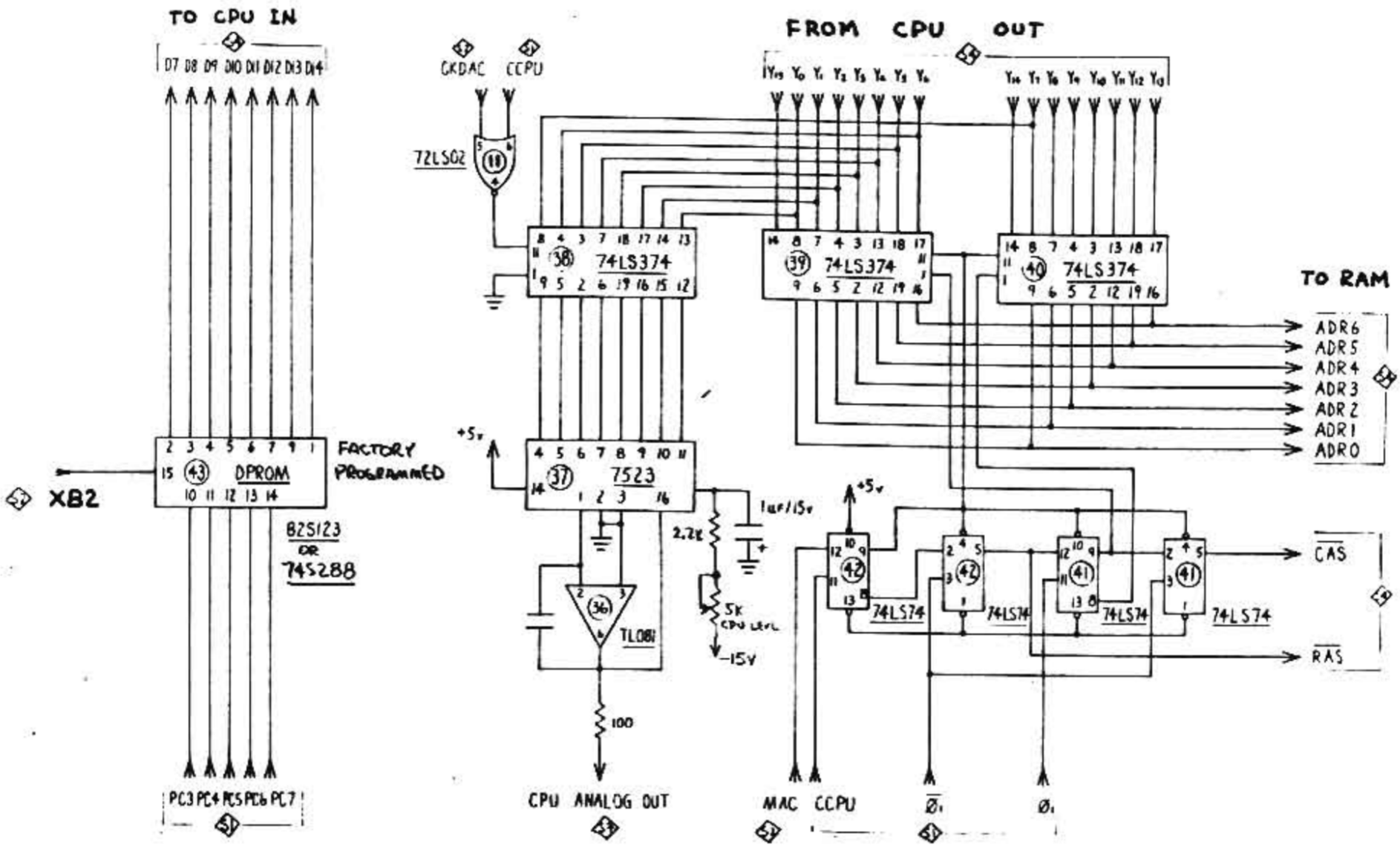
MAIN OUTPUT REFERENCE VOLTAGE
AND DELAY ONLY DAC

HD 921 REV. C,D
SHEET 7 OF 7



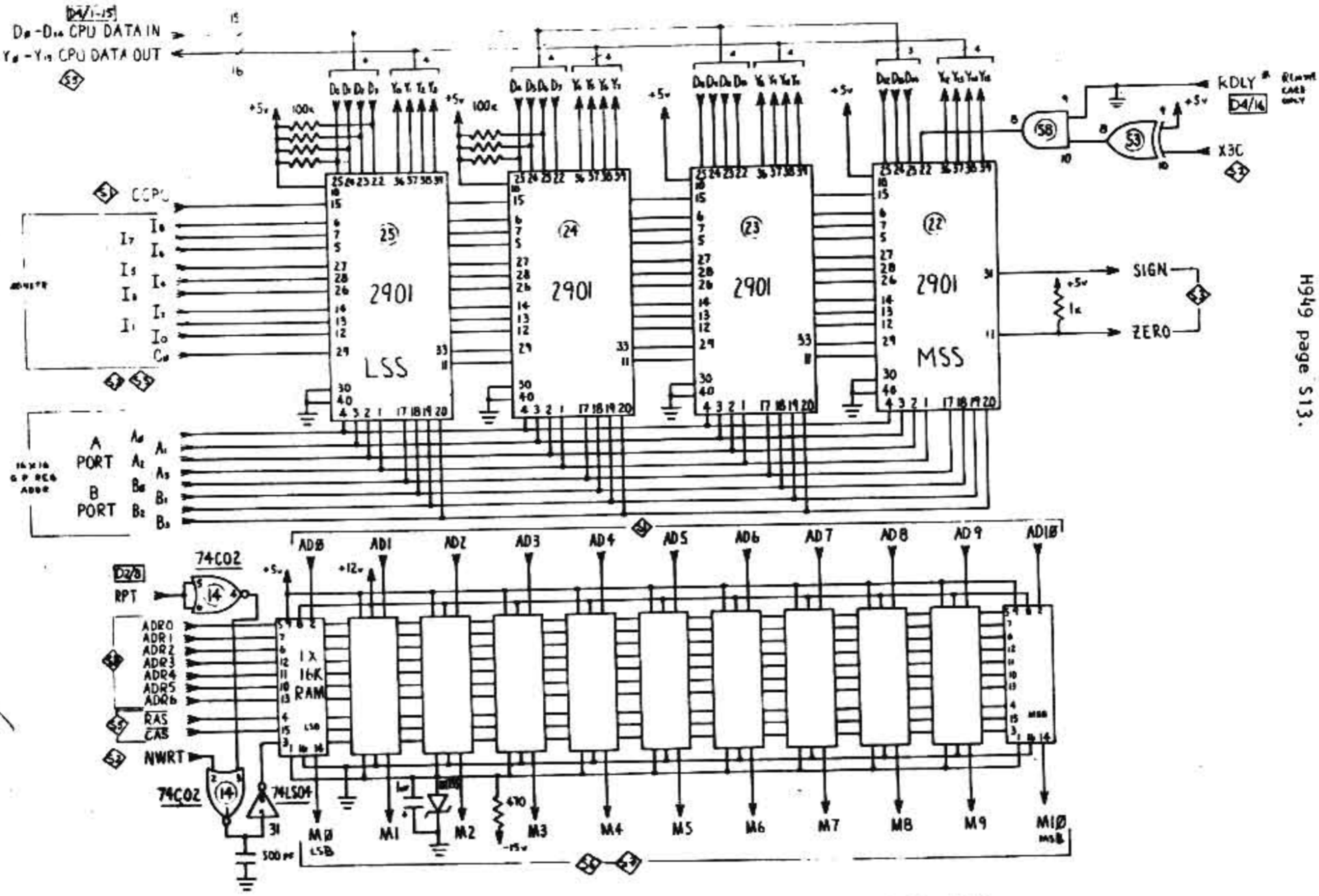
FIFO ARRAY AND TIMING,
MAIN OUTPUT DAC

HD 921 REV. C,D SHEET 6 OF 7



DATA PROM, CPU ANALOG OUT AND RAM ADDRESS AND TIMING

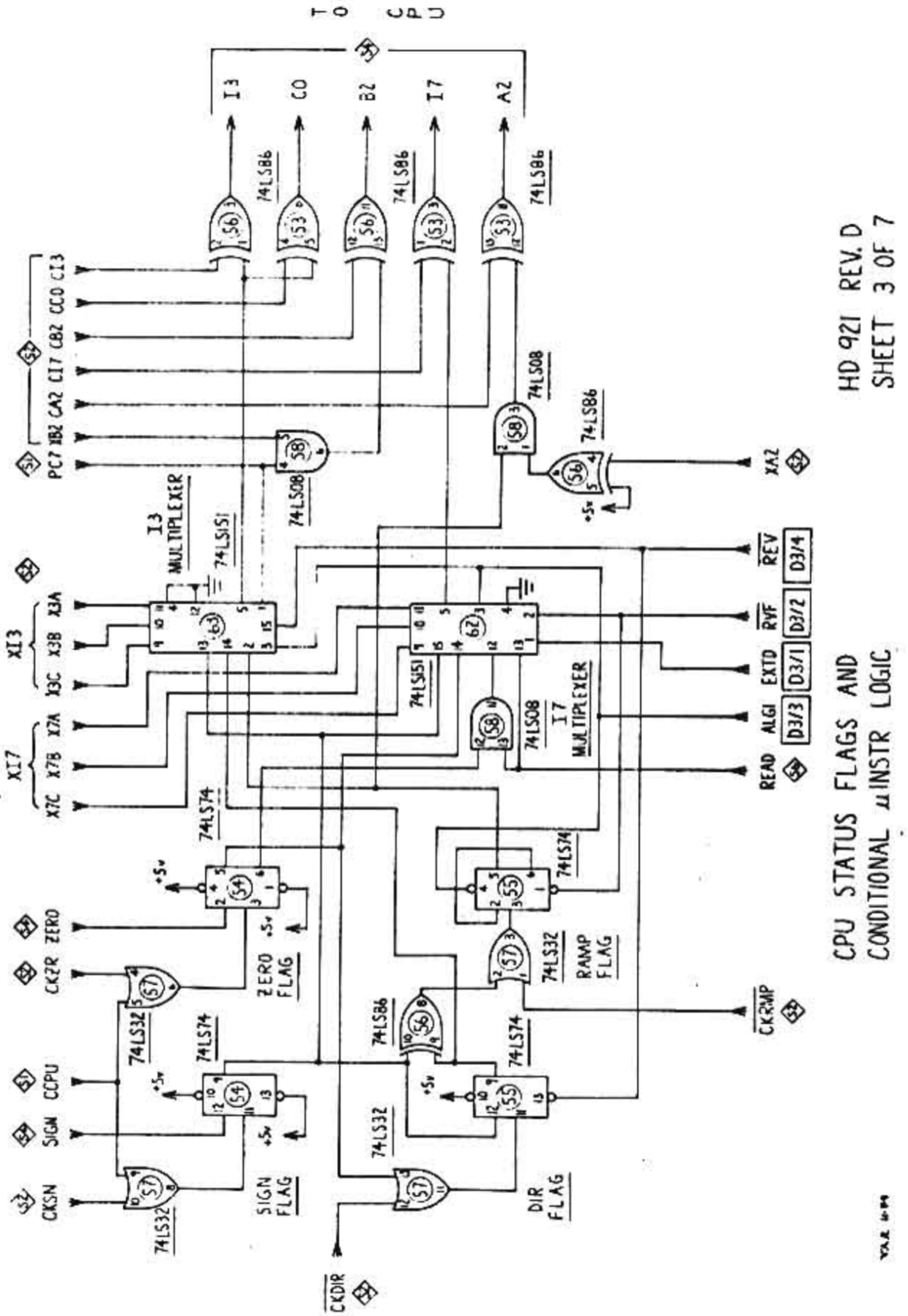
HD 921 REV. C.D
SHEET 5 OF 7



16-BIT CENTRAL PROCESSING UNIT (CPU) AND
11 x 16K DYNAMIC RANDOM ACCESS MEMORY ARRAY (RAM)

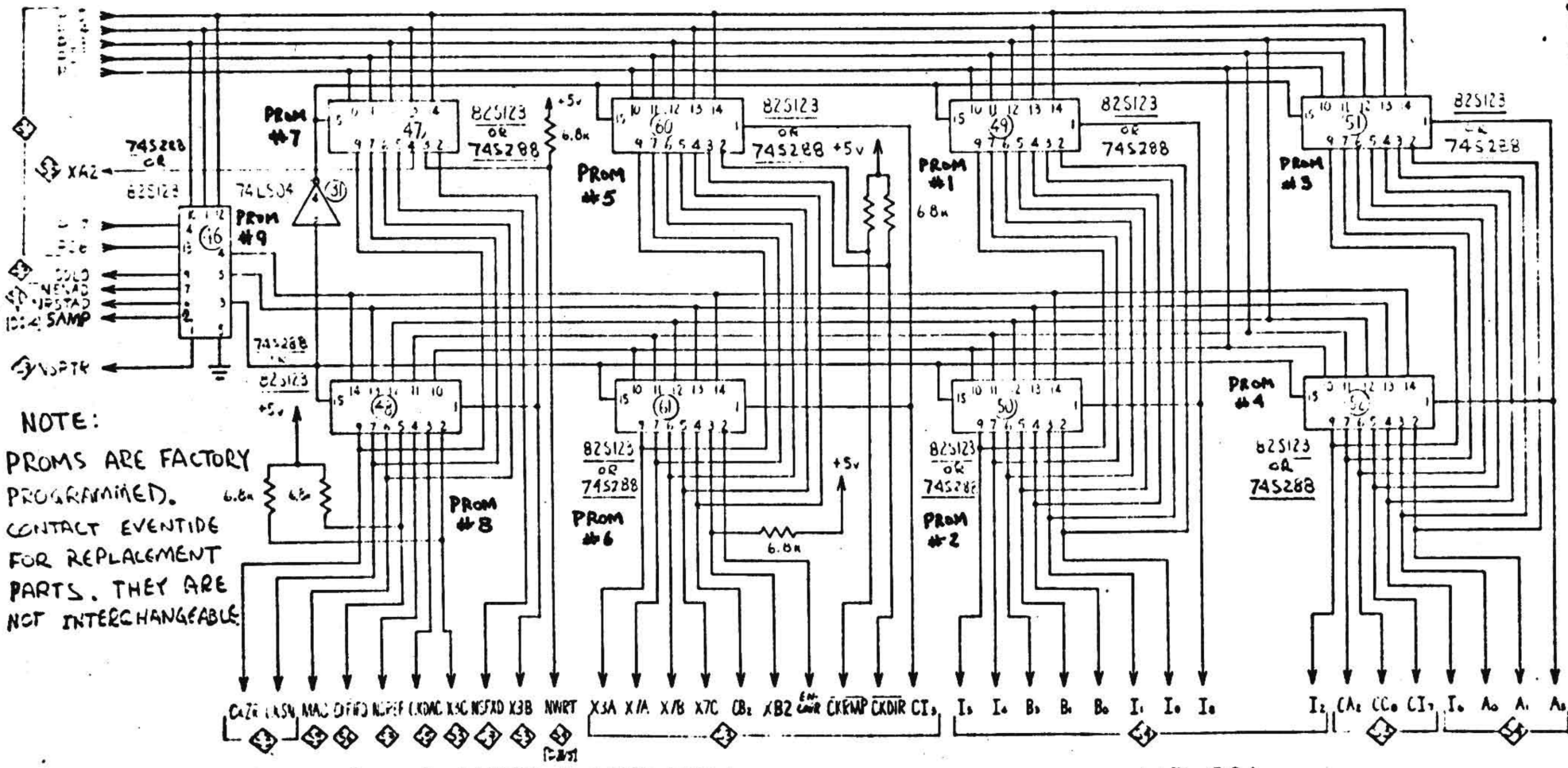
HD 921 REV.C,D
SHEET 4 OF 7

H949 page S13.



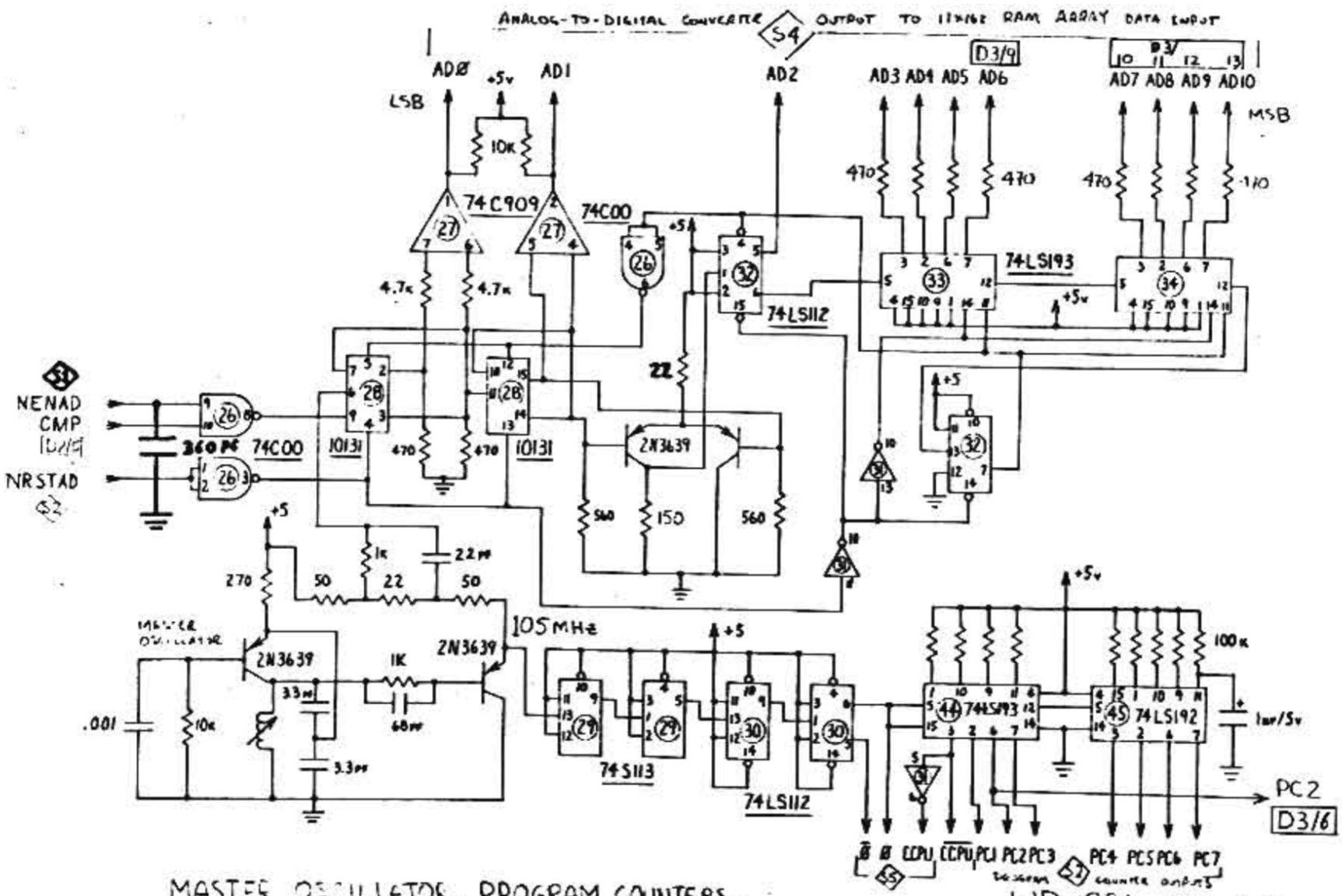
HD 921 REV. D
SHEET 3 OF 7

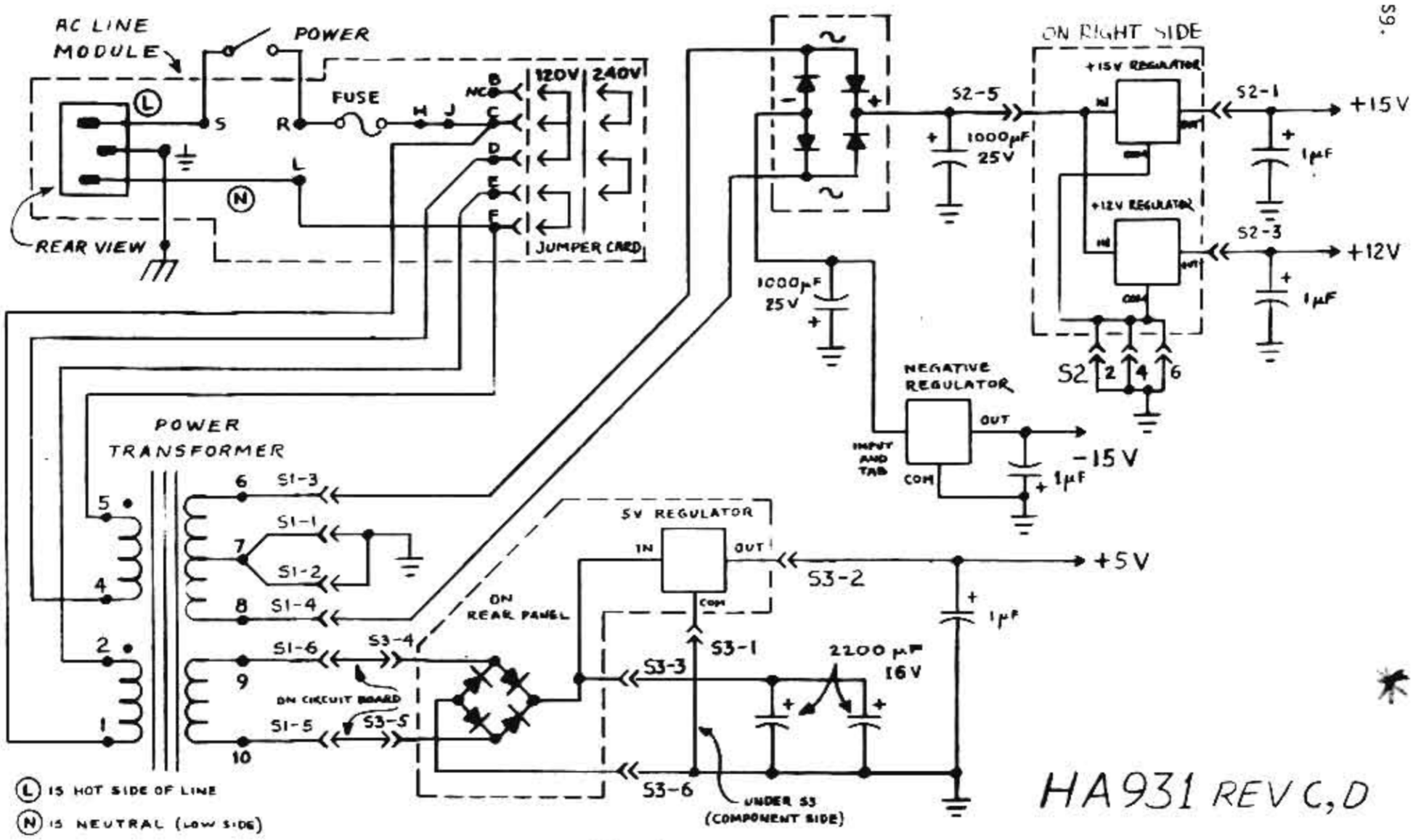
CPU STATUS FLAGS AND
CONDITIONAL μINSTR LOGIC



TIMING AND MICRO-INSTRUCTION
PROGRAMMABLE READ-ONLY-MEMORIES (PROMS)

HD 921 REV. D
SHEET 2 OF 7


ANALOG-TO-DIGITAL CONVERTER
S4
OUTPUT TO 11X16 RAM ARRAY DATA INPUT
AD0
AD1
AD2
AD3 AD4 AD5 AD6
AD7 AD8 AD9 AD10
LSB
MSB
+5v
10K
74C909
74C00
74LS112
74LS193
74LS192
74LS113
470
4.7K
22
560
150
2N3639
NENAD CMP
NRSTAD
360 PF
10131
270
50
1K
22 PF
105 MHz
33 PF
68 PF
3.3 PF
.001
100K
1uF/5v
PC2
D3/6
MASTER OSCILLATOR, PROGRAM COUNTERS, AND ANALOG-TO-DIGITAL CONVERTER
HD 921 REV. C.D
SHEET 1 OF 7

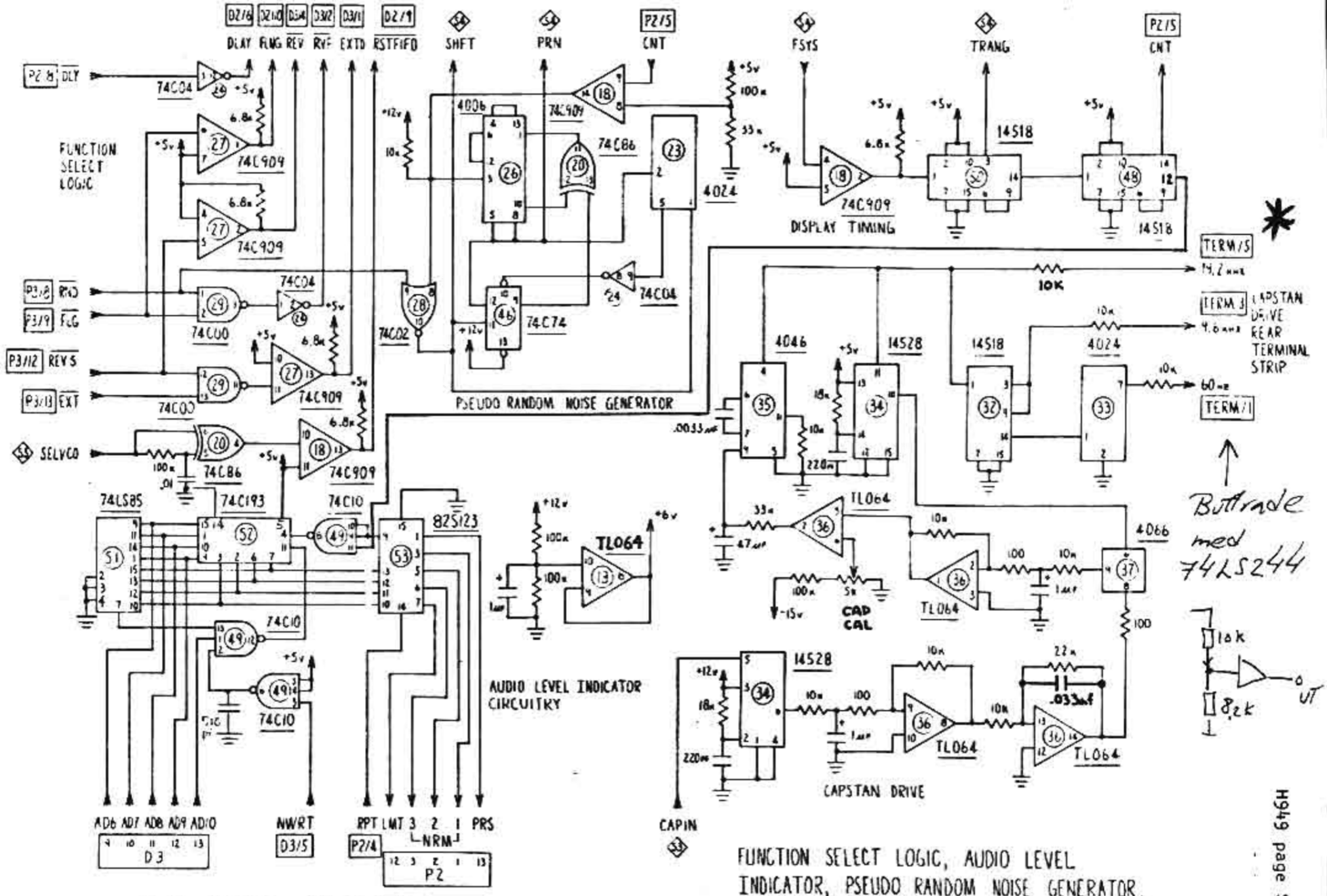


HA931 REV C,D

POWER SUPPLY

SHEET 6 OF 6

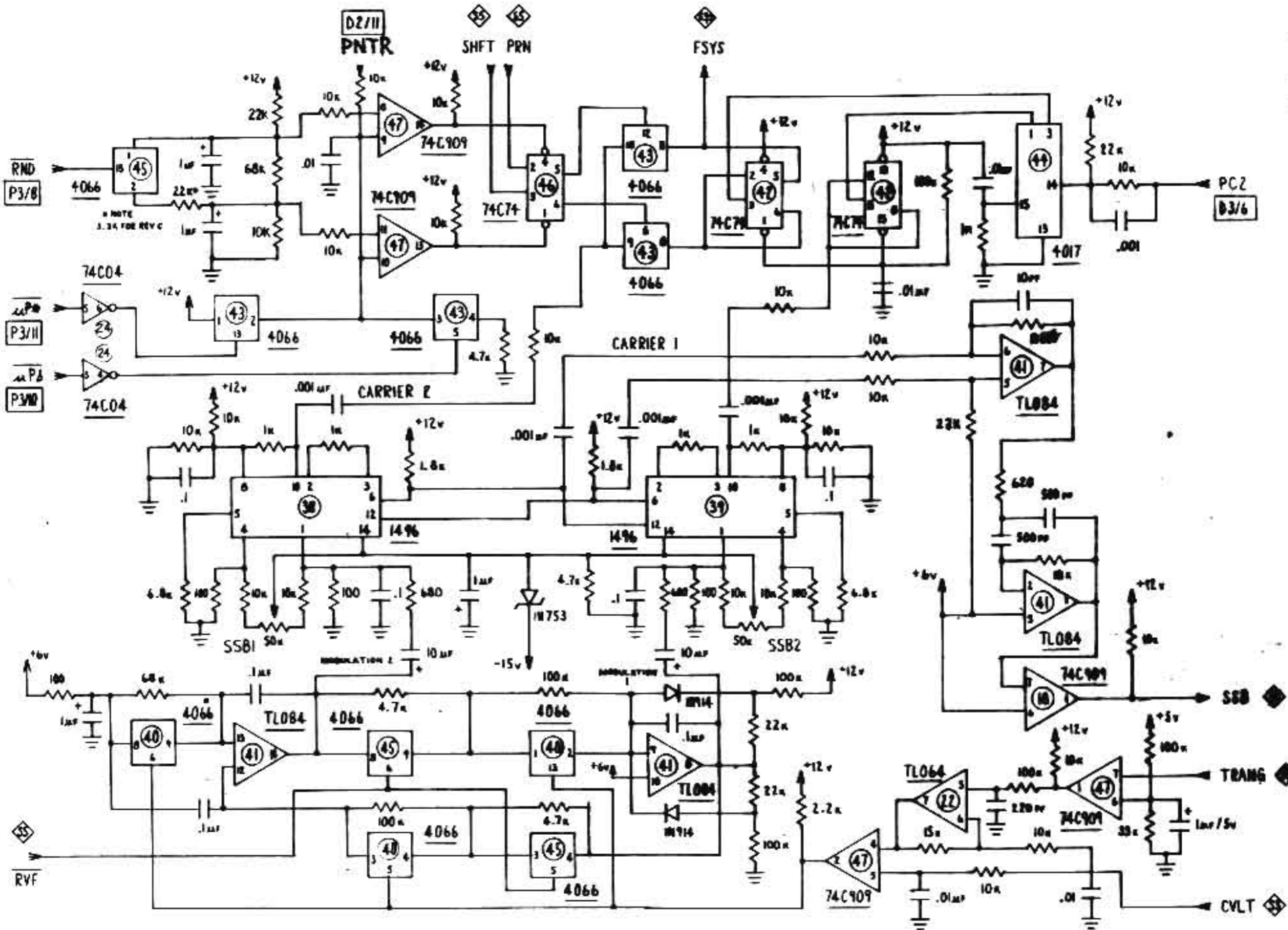
AB · 1979



HA 931 REV. C,D SHEET 5 OF 6

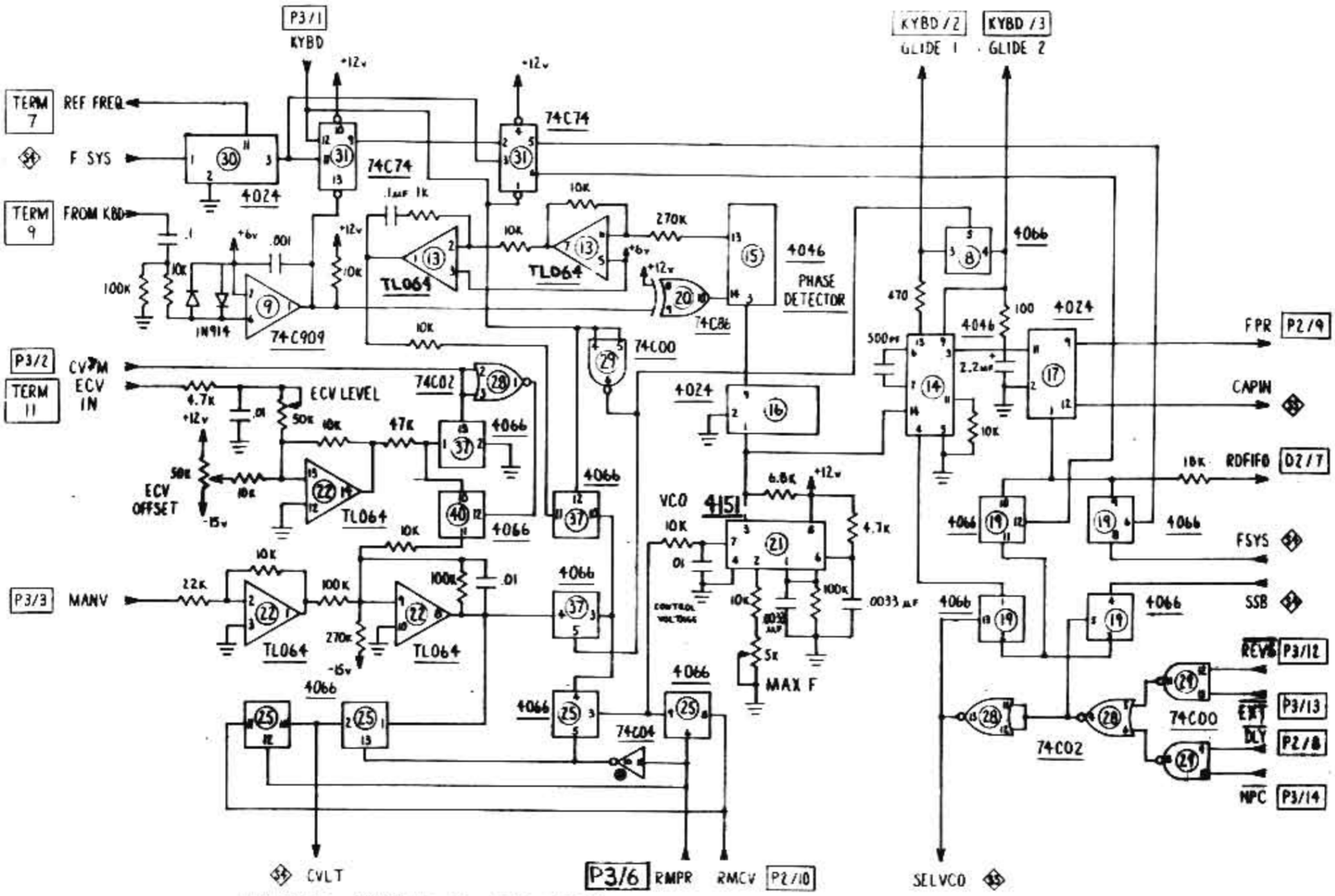
FUNCTION SELECT LOGIC, AUDIO LEVEL INDICATOR, PSEUDO RANDOM NOISE GENERATOR, CAPSTAN DRIVE AND DISPLAY TIMING CIRCUITRY

H949 page 58.



SINGLE SIDE BAND GENERATOR

HA931 REV. C, D SHEET 4 OF 6



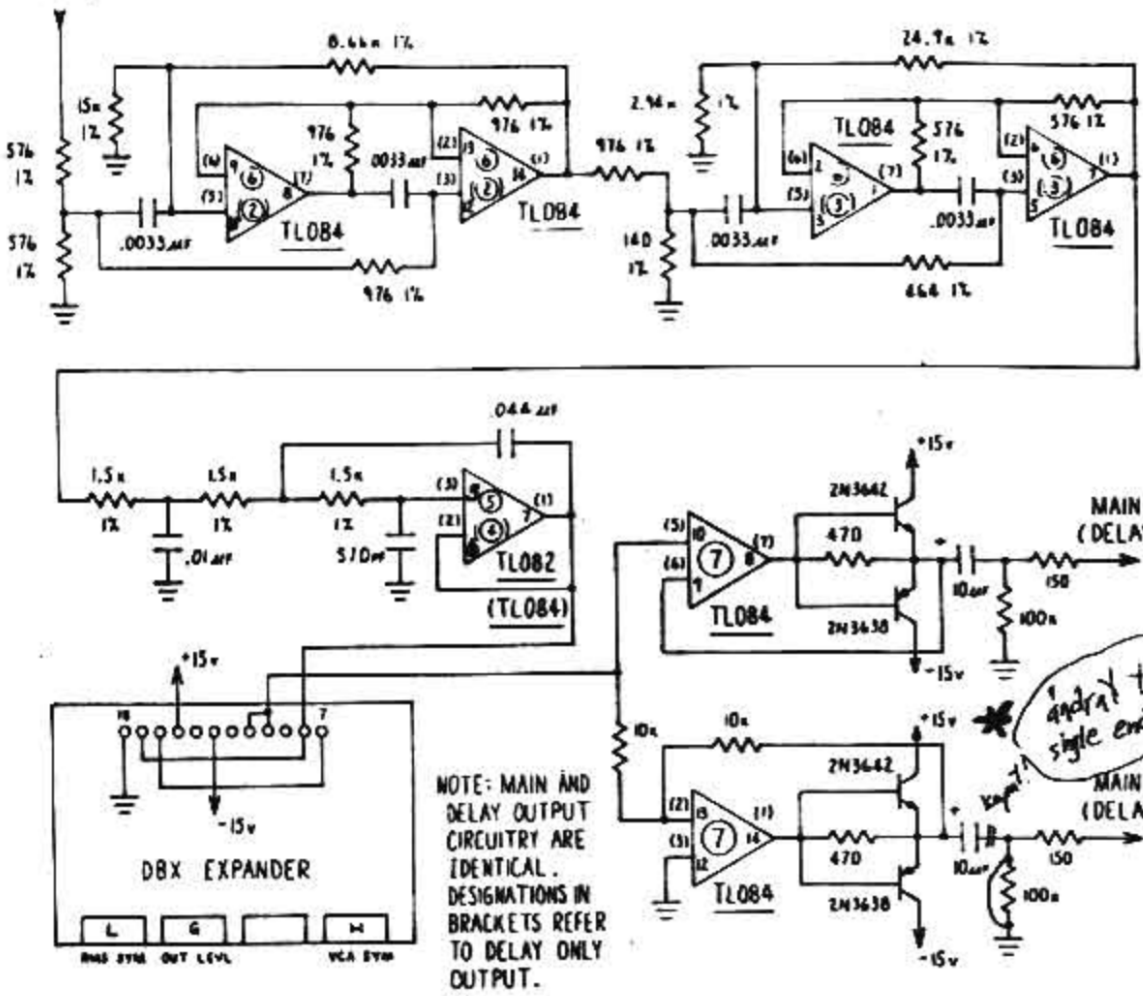
VOLTAGE CONTROLLED OSCILLATOR
AND READ FIFO CLOCK SELECT

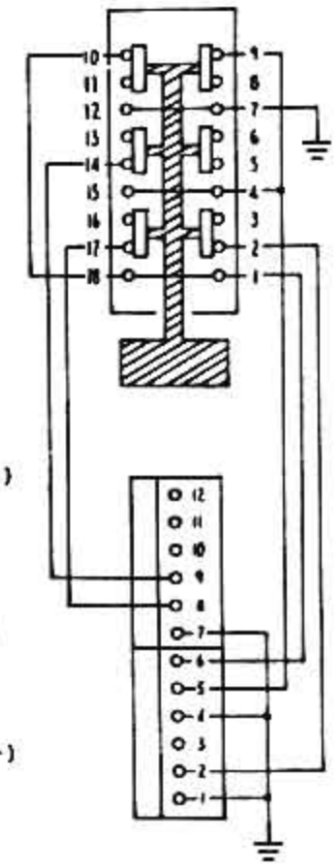
HA 931 REV. C,D
SHEET 3 OF 6

YAS 11-79

H949 page 9.

DZ/14 MDAC
(Z) (DDAC)





LINE SWITCH

6 POLE / DOUBLE THROW PUSH - PULL SWITCH

AUDIO I/O

MOLEX SOCKET

PIN ASSIGNMENTS

PIN #	SIGNAL	
1	GND	
2	COM	DELAY ONLY XLR
3	+	DELAY ONLY XLR
4	GND	
5	+	AUDIO IN XLR
6	COM	AUDIO IN XLR
7	GND	
8	COM	MAIN OUT XLR
9	+	MAIN OUT XLR

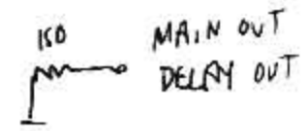
YOKOHAMA 11-79

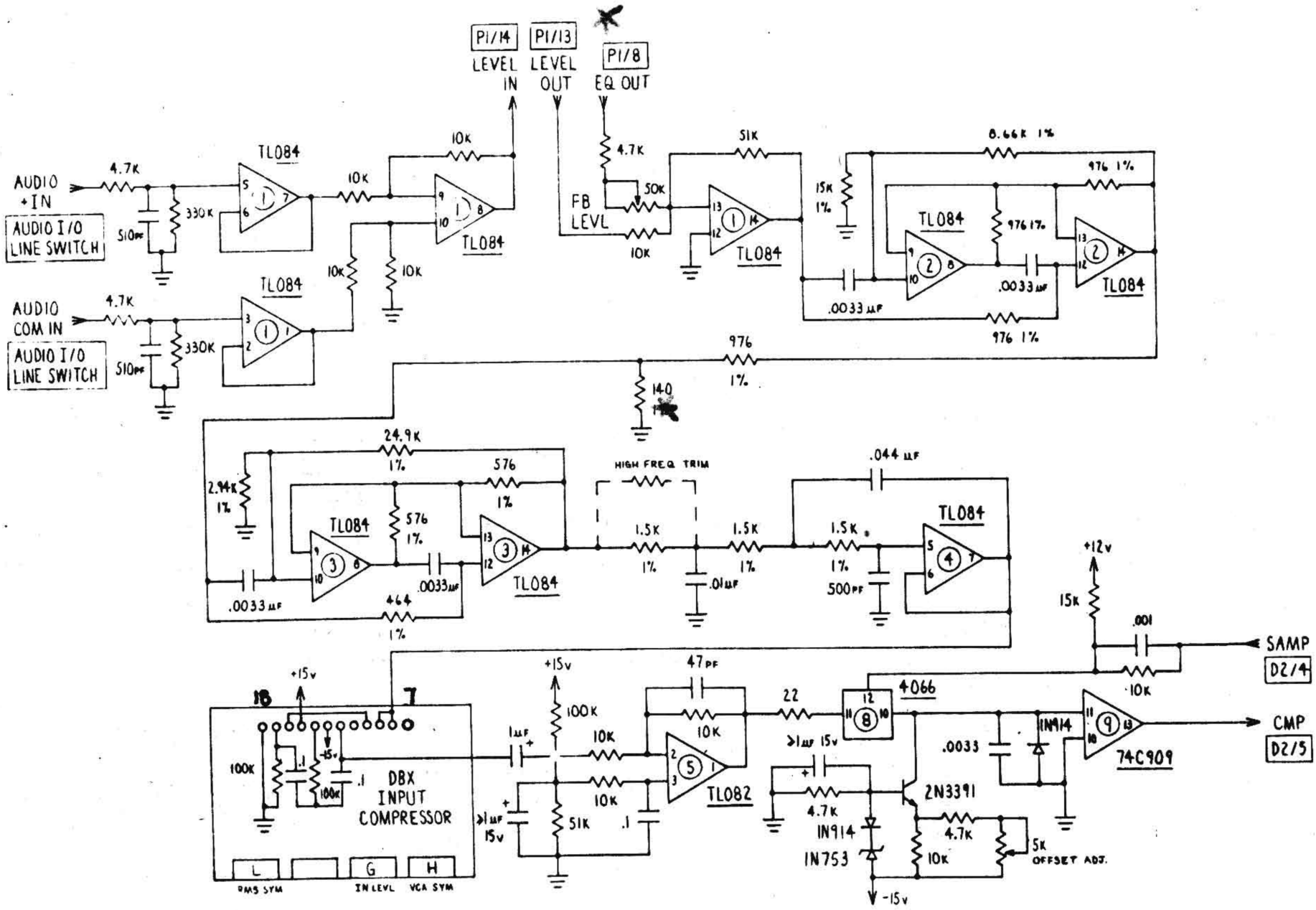
OUTPUT AUDIO PROCESSING

HA 931 REV. C,D SHEET 2 OF 6

* OBS Andra

83.08.25 GS

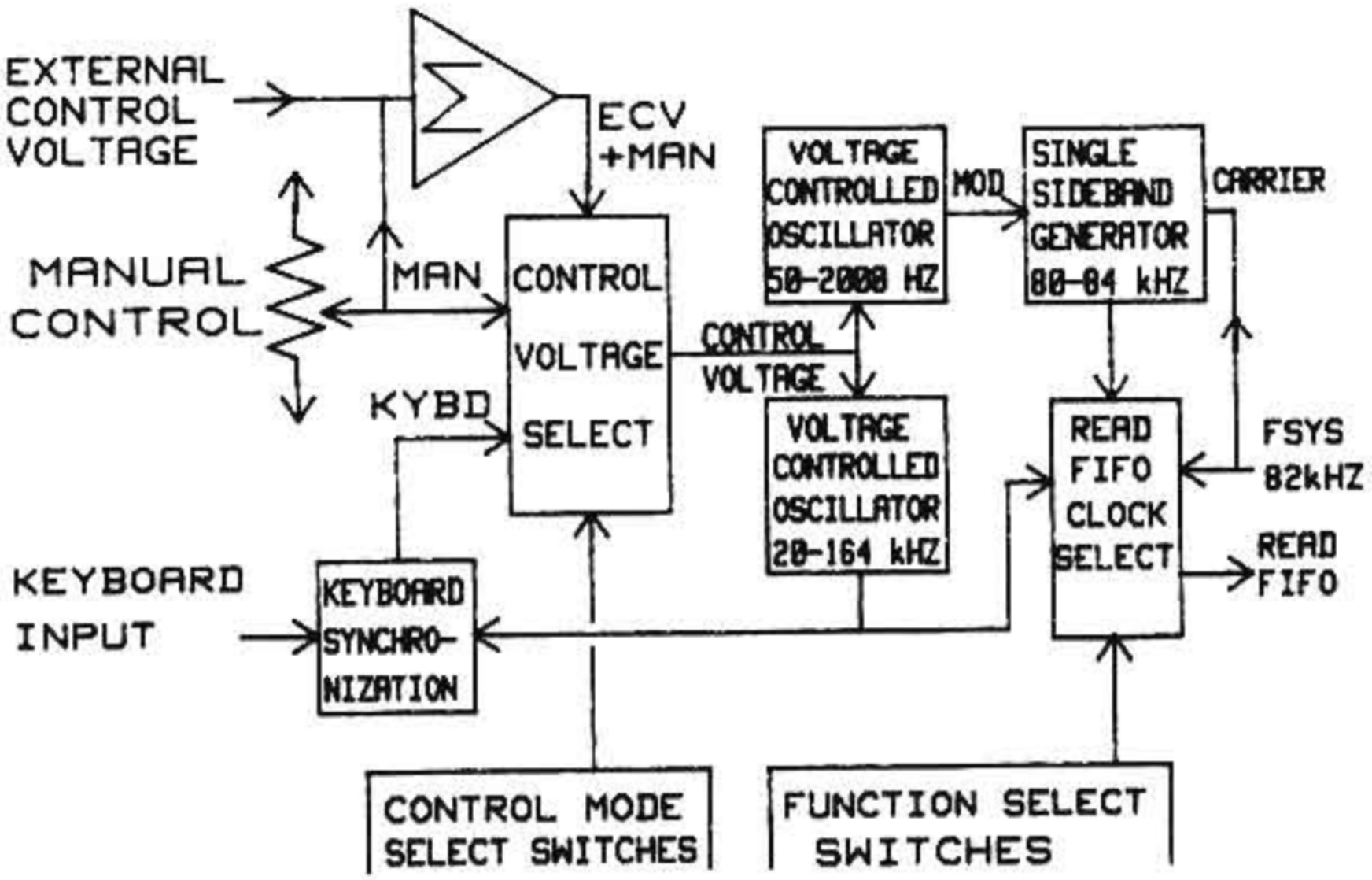




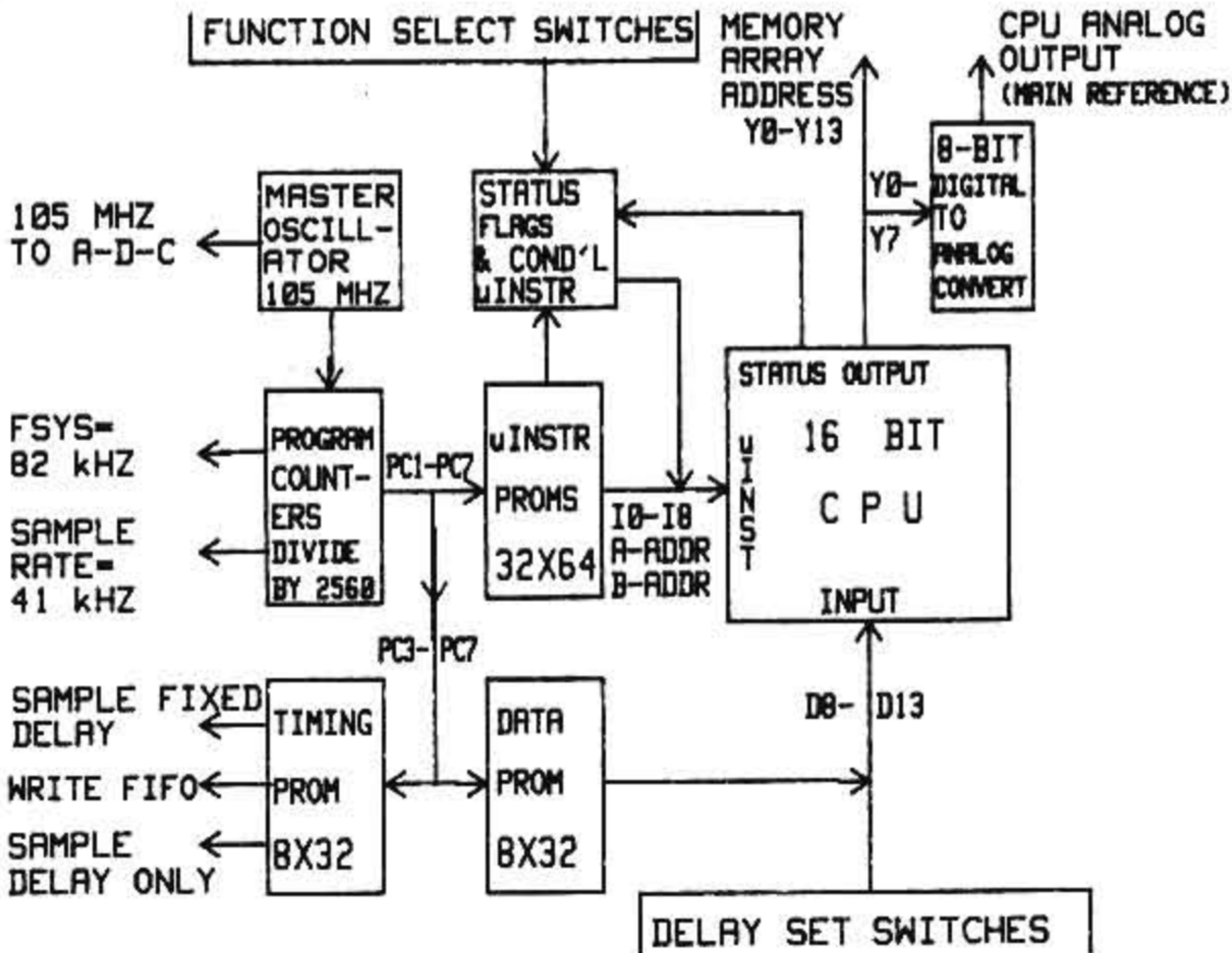
INPUT AUDIO PROCESSING

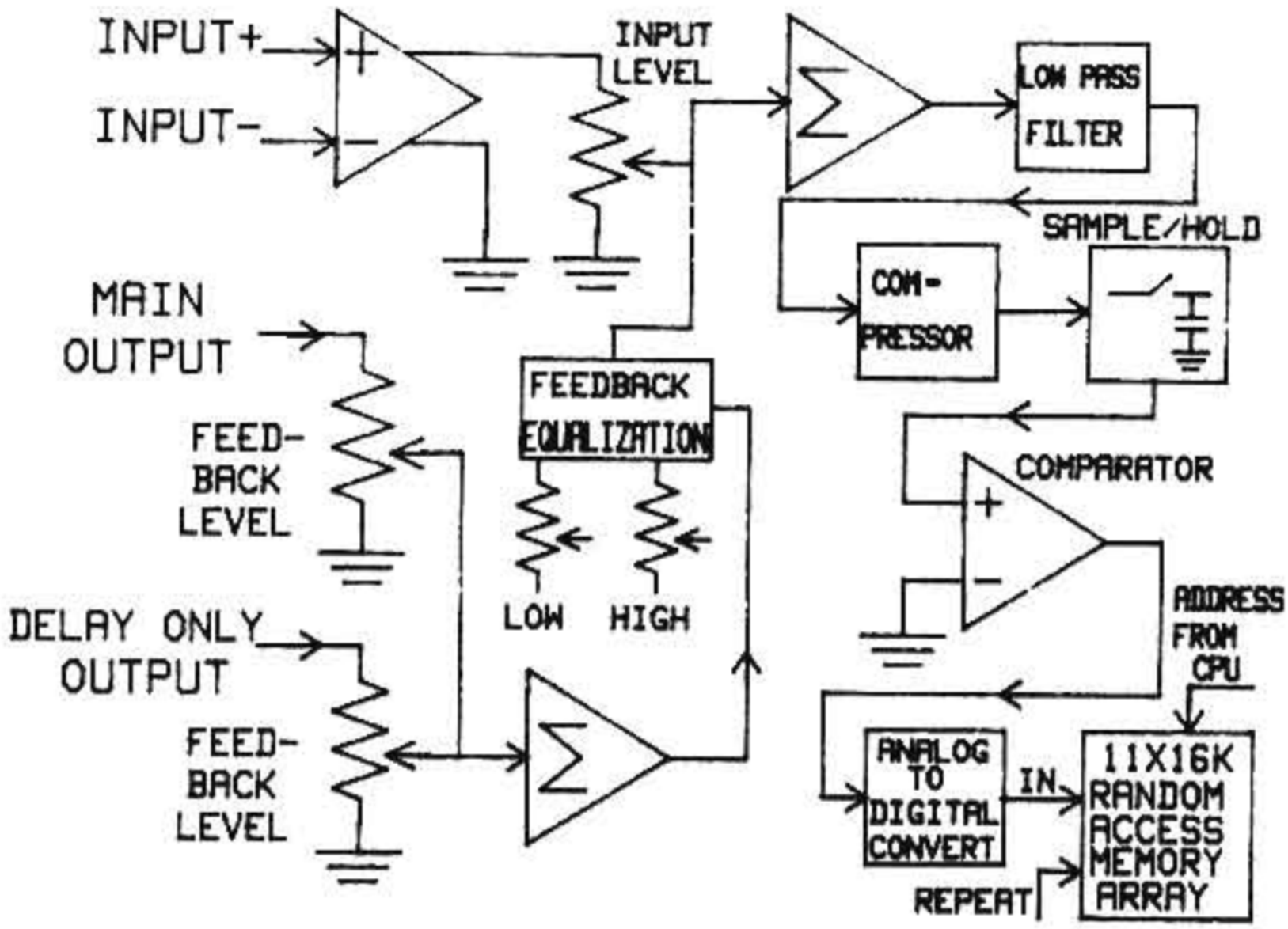
HA 931 REV. C,D
SHEET 1 OF 6

VCA R 11-79

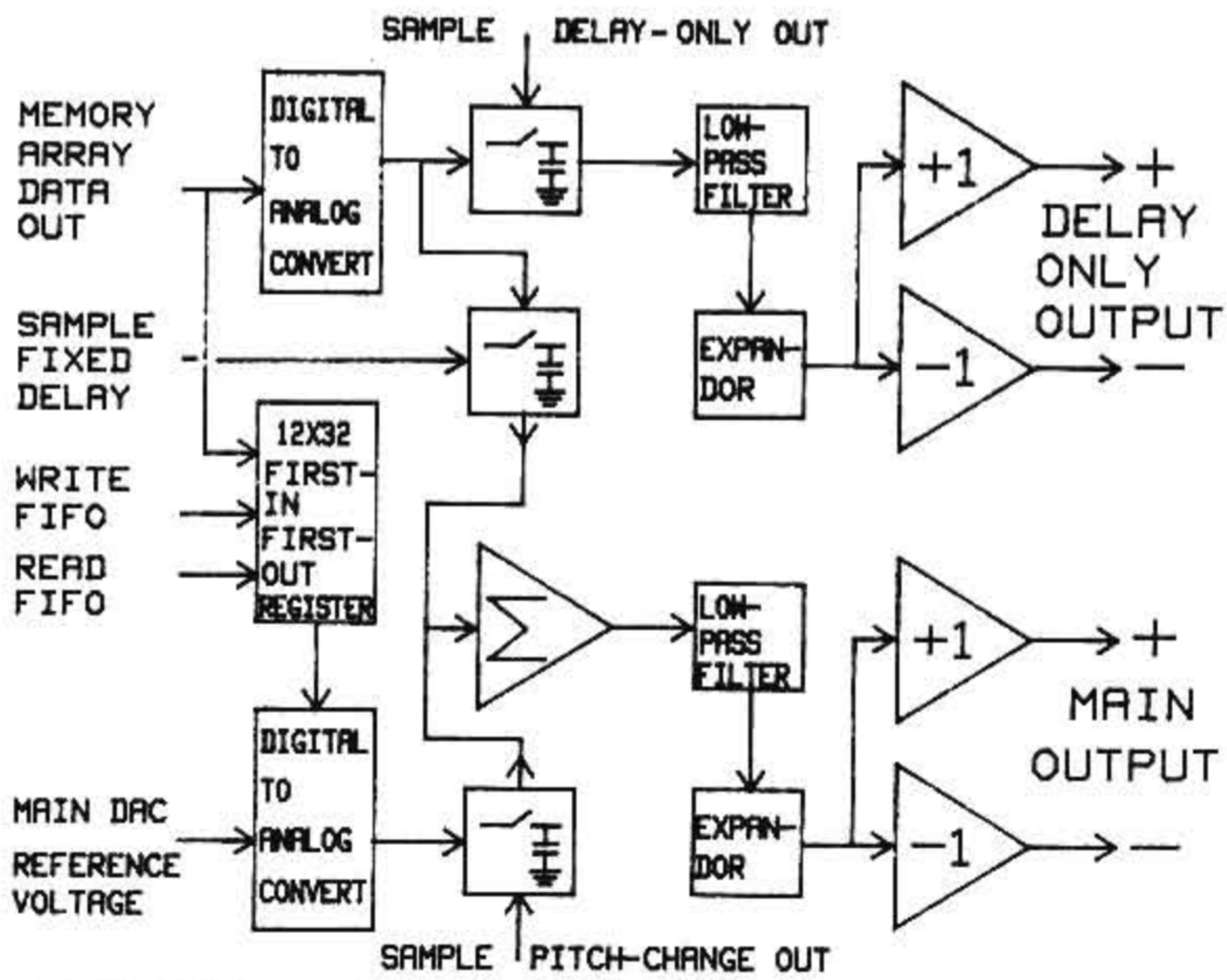


PITCH CHANGE TIMING & CONTROL





INPUT AUDIO PROCESSING



OUTPUT AUDIO PROCESSING

MASTER BLOCK DIAGRAM