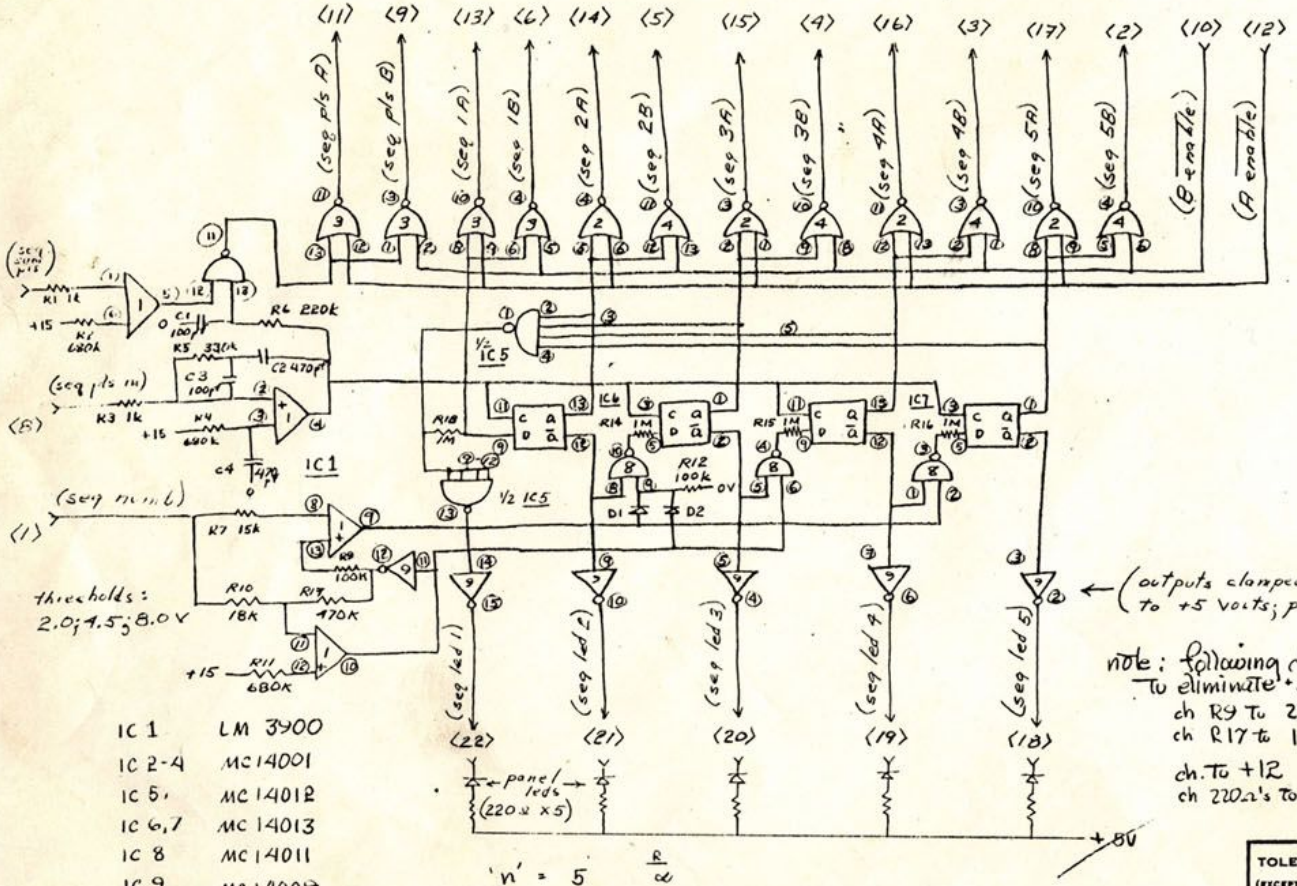
DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
3/11		[illegible]			
		[illegible]			
		RB, 13			

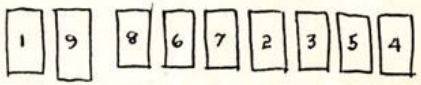
(in future consider running leds from +12V, changing IC 9, R9, 13 and panel R's appropriately)



(outputs clamped to +5 volts; pin 1)

(23) (OPEN; feedthru on m.b. to (J))
(24) (N)
(25) +15V
(26) +5V
(27) (OPEN; feedthru on m.b. to A enable)
(28) to (30) (OPEN)

IC layout



note: following changes to eliminate +5V sup:
ch R9 to 220k
ch R17 to 1.2 meg.
ch. to +12
ch 220Ω's to 680Ω

IC 1	LM 3900
IC 2-4	MC14001
IC 5,	MC14012
IC 6,7	MC14013
IC 8	MC14011
IC 9	MC14009

all grounds to (N)

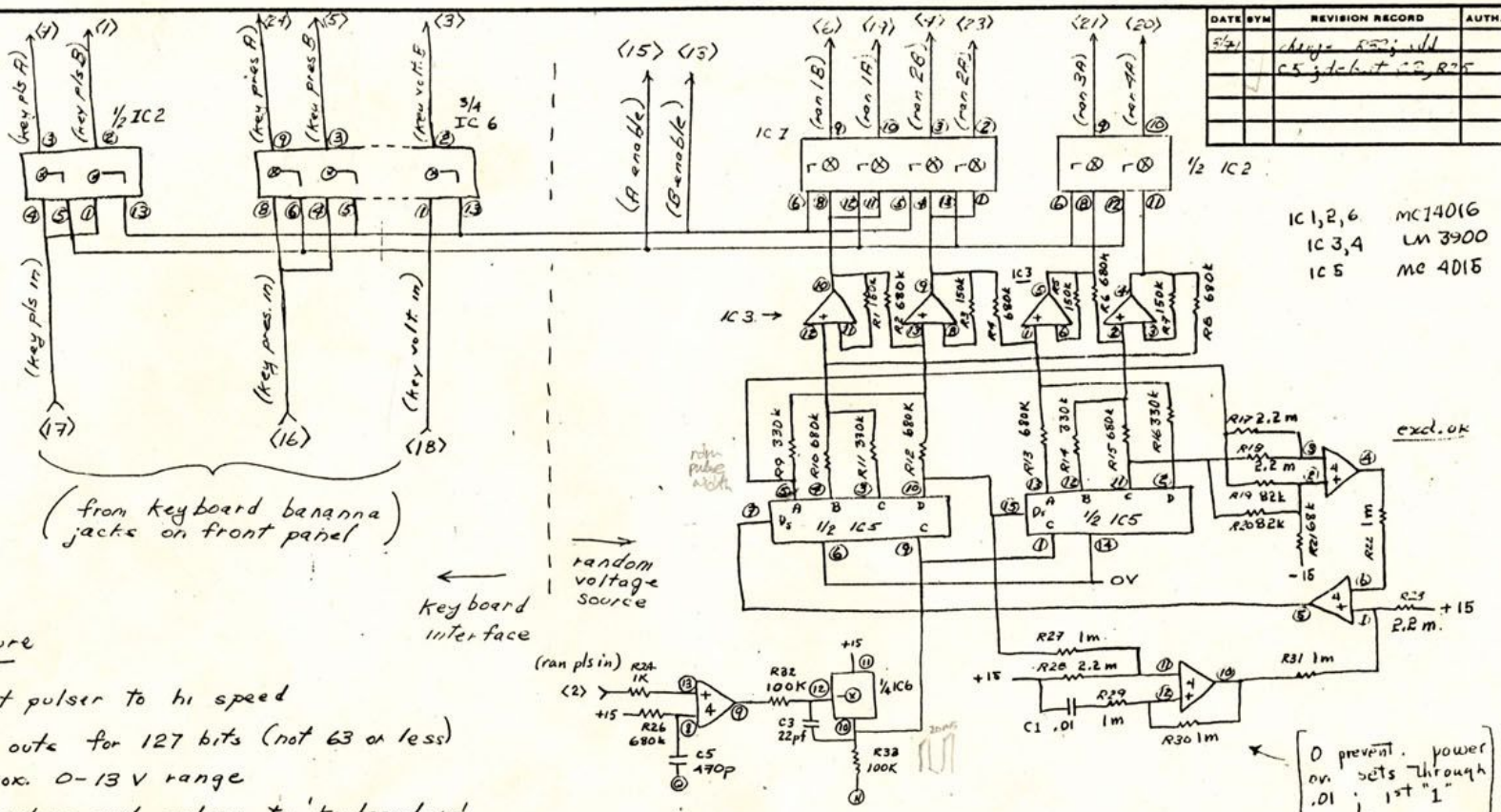
'n' =	Ω
5	
4	390k
3	200k
2	120k
pulsed	390k

last R - 18 no RB, 13
last c - 4

TOLERANCES (EXCEPT AS NOTED)	BUCHLA & ASSOCIATES		
DECIMAL ±	series 200	SCALE	DRAWN BY / APPROVED BY
FRACTIONAL ±	TITLE SCH; 5 STAGE SEQ		PART OF 208 P.S.S.
ANGULAR ±	DATE 3-30-73	DRAWING NUMBER B 2080-1A	

K&E ALBANENE 10 8468 ENGINEERS' STANDARD PAPER

MADE IN U.S.A. 88100



IC 1,2,6 MC14016
IC 3,4 LM 3900
IC 5 MC 4015

DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
5/21		change R33 to 68K C5 to 470pf, R25			

Test procedure

input: pulser; set pulser to hi speed

test: 4 random outs for 127 bits (not 63 or less) and approx. 0–13 V range

connect randoms and pulser to 'keyboard-in' signals. Test program card for presence of key pulse, key pressure, key voltage, random 1, random 2.

test same with program sw. on 'both' and 'front panel' with p.s. @ 16 V

(8) (OPEN; feedthru on mother board for B enable)
(9) (OPEN; " " " " " B enable)
(10) (OPEN; " " " " " env. attack pot)
(11) +15V
(12) (OPEN)
(14) −15V.
(22) ⓖ

04 .01

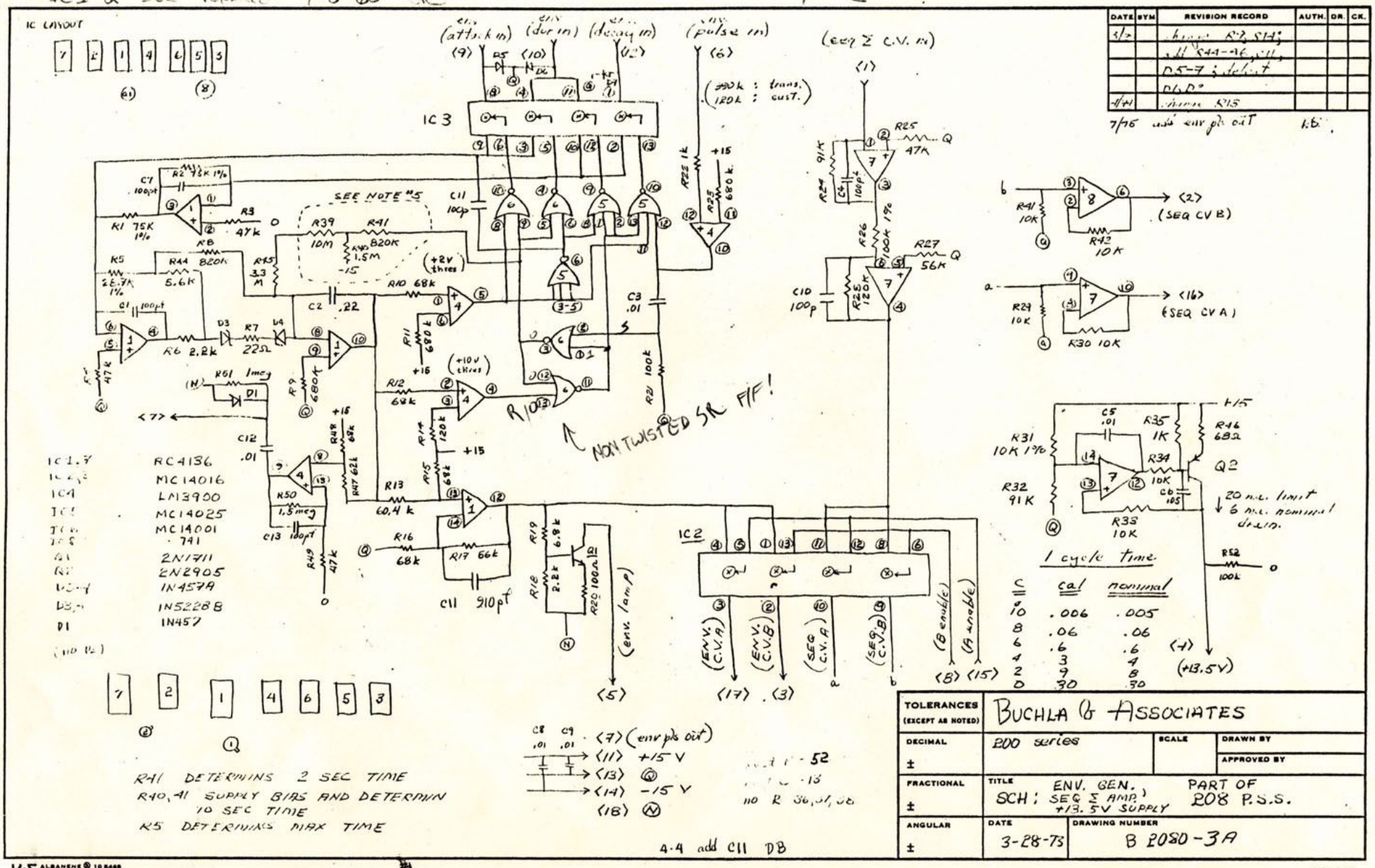
IC layout: 4 5 3 2 1 6

last R 33 no R25
last C 5 no C2

TOLERANCES (EXCEPT AS NOTED)	BUCHLA & ASSOCIATES		
DECIMAL ±	200 series	SCALE	DRAWN BY / APPROVED BY
FRACTIONAL ±	TITLE SCH: RANDOM VOLT. SOURCE, KEYBOARD INTERFACE		PART OF 208 P.S.
ANGULAR ±	DATE 3-28-73	DRAWING NUMBER B 2080-2A	

IC1 & IC2 replaced 7-8-80 dk

3

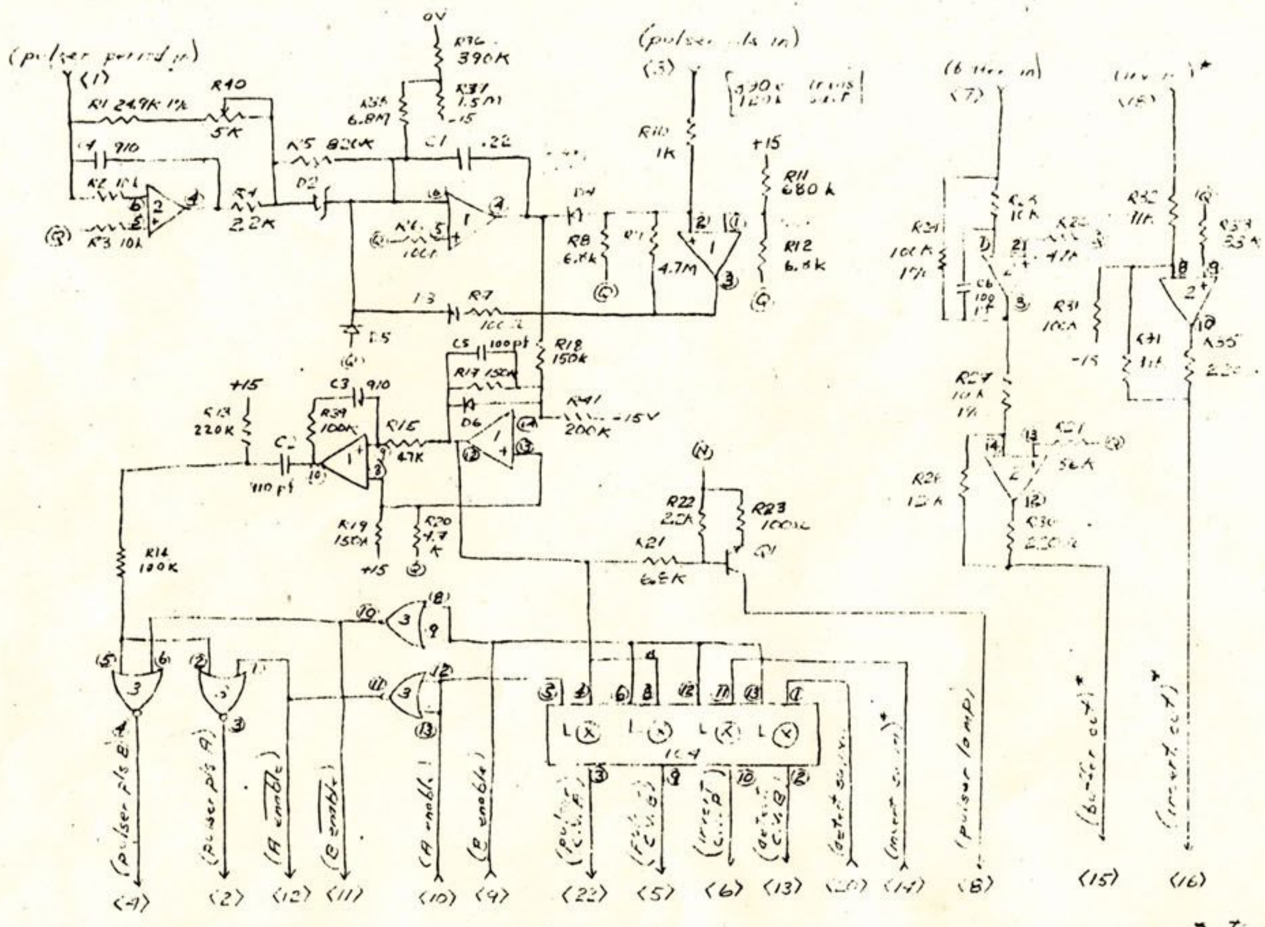


DATE	BYM	REVISION RECORD	AUTH.	DR.	CK.
3/2		change R-2 SHJ			
		add R44-46, C11,			
		D5-7; delete			
		D1, D2			
4/11		change R15			

7/15 add env pls out K.B.

TOLERANCES (EXCEPT AS NOTED)	BUCHLA & ASSOCIATES		
DECIMAL ±	200 series	SCALE	DRAWN BY / APPROVED BY
FRACTIONAL ±	TITLE ENV. GEN. SCH; SEQ Σ AMP. +13.5V SUPPLY	PART OF 208 P.S.S.	
ANGULAR ±	DATE 3-28-75	DRAWING NUMBER B 2080-3A	

DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
3/74		change R4,5,36,38,			
		R13 to 715; add R			
		37,41; delete D1			
1/74		change R2?; add R[illegible]			
		[illegible]			



C	cal	nominal actual	freq loop	adj for
10	.002	.0022	450	.002-.0025
8	.02	.015	65	
6	.2	.15	6.5	
4	1	1.3		
2	3	3		
0	10	10		

* to panel only

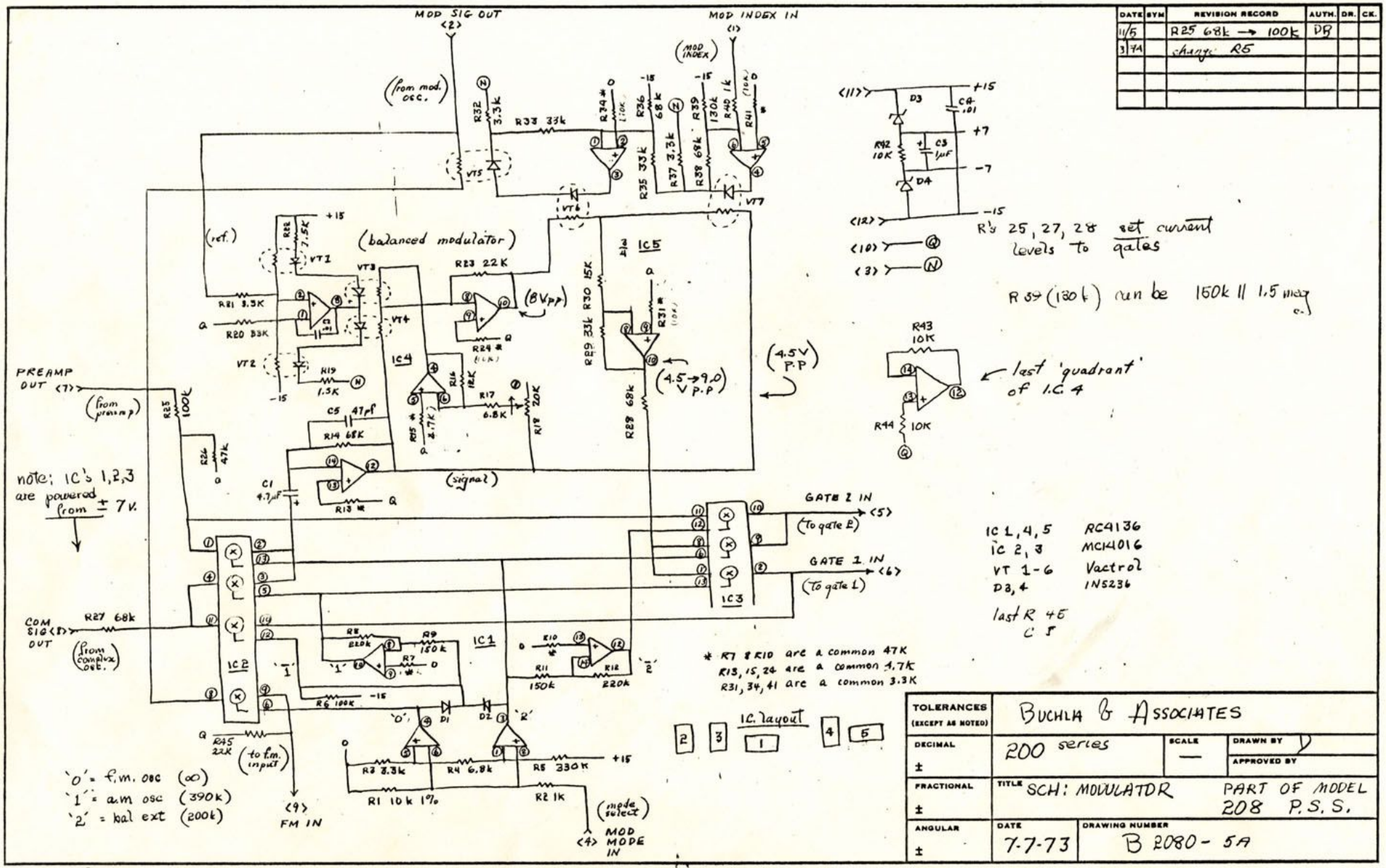
IC 1,2 RC4156
IC 3 MC14001
IC 4 MC14016
D3-6 1N457
D2 1N3224B
Q1 2N1711
no D1

C8 .01 → (17) Ⓠ
(19) (feedthru)
→ (21) -15V
(23) Ⓝ
→ (24) +15V
C7 .01

last R: 41
last C: 8

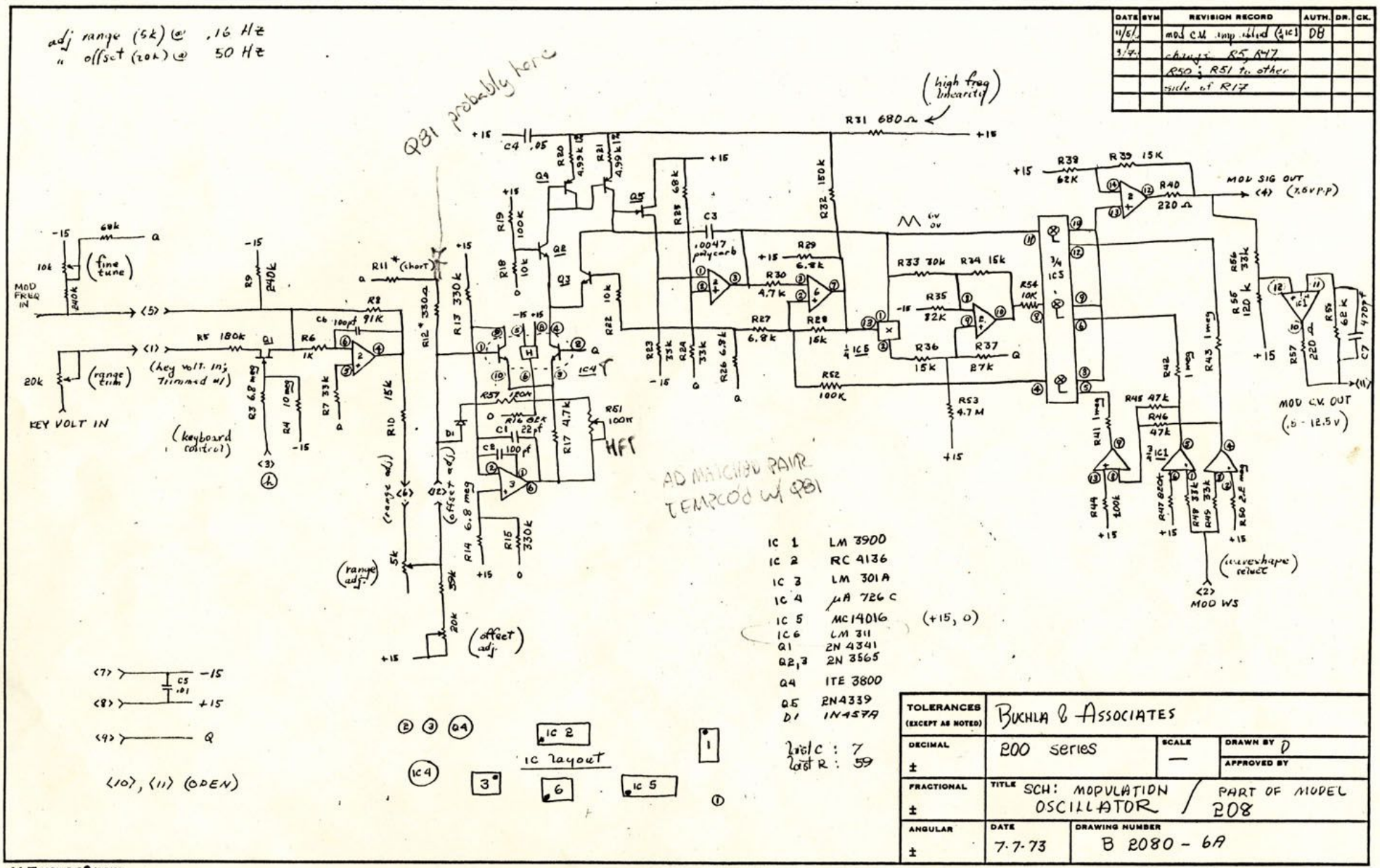
IC layout
1 2 4 3
①

TOLERANCES (EXCEPT AS NOTED)	BUCHLA + ASSOC		
DECIMAL ±	200 SERIES	SCALE —	DRAWN BY B H / APPROVED BY
FRACTIONAL ±	TITLE ECHO: PULSER, BUFFER, INVERTER	PART OF 208 P.S.S.	
ANGULAR ±	DATE 6/5/75	DRAWING NUMBER B2080-4A	



DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
11/5		R25 68k → 100k	DB		
3/74		change R5			

TOLERANCES (EXCEPT AS NOTED)	BUCHLA & ASSOCIATES		
DECIMAL ±	200 series	SCALE —	DRAWN BY / APPROVED BY
FRACTIONAL ±	TITLE SCH: MODULATOR		PART OF MODEL 208 P.S.S.
ANGULAR ±	DATE 7-7-73	DRAWING NUMBER B 2080 - 5A	

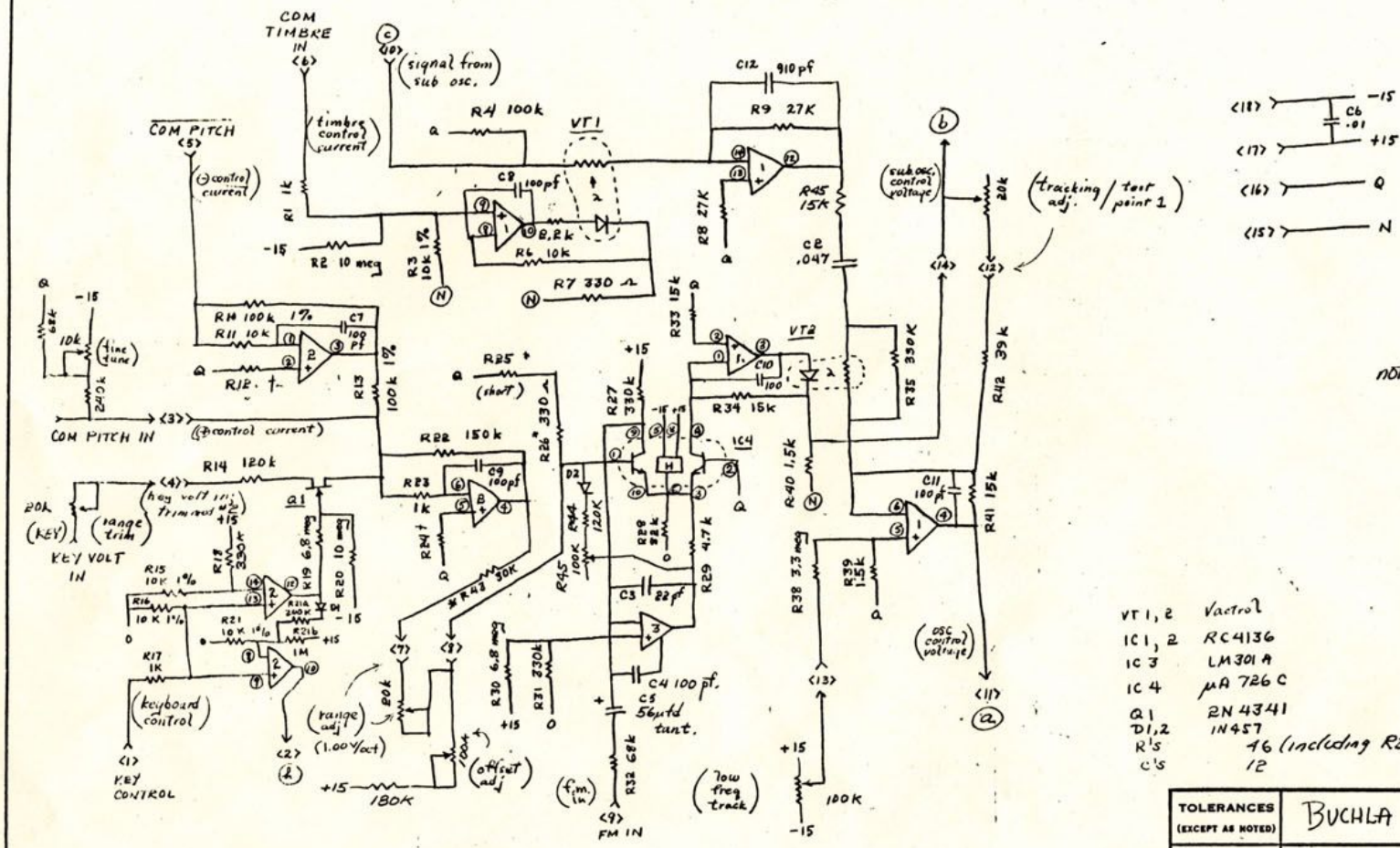


DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
11/6/		mod CM implemented (½IC)	DB		
3/7/		changes R5, R47			
		R50; R51 to other			
		side of R17			

TOLERANCES (EXCEPT AS NOTED)	BUCHLA & ASSOCIATES		
DECIMAL ±	200 series	SCALE —	DRAWN BY D / APPROVED BY
FRACTIONAL ±	TITLE SCH: MODULATION OSCILLATOR / PART OF MODEL 208		
ANGULAR ±	DATE 7-7-73	DRAWING NUMBER B 2080 - 6A	

DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
3/74		change 'offset adj'			
		R on mod. add R45			
		change R18			

(osc. control voltage generator)



note complex osc. is spread out on 3 boards; interconnections are coded with letters (a) - (g).

see also B 2080 - 8
B 2080 - 9

VT 1, 2	Vactrol
IC 1, 2	RC4136
IC 3	LM301A
IC 4	μA 726 C
Q1	2N4341
D1, 2	IN457
R's	46 (including R21a)
C's	12

OBS

4 trim pots (all off board)

con't	
5	mod key
6	osc key
9	both

Layout

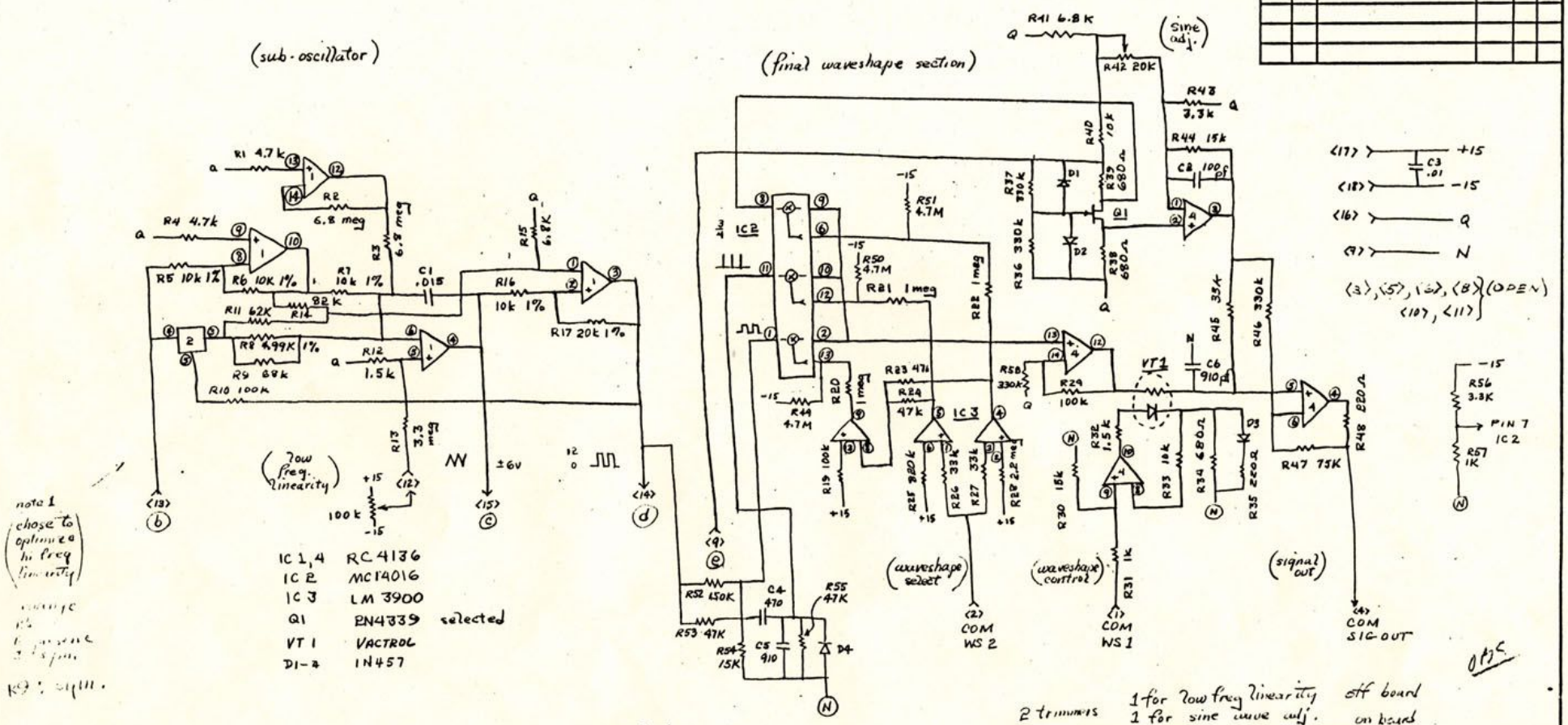
† R12 and R24 are common 22K no C1

* R43 is 39K in unit #4

TOLERANCES (EXCEPT AS NOTED)	BUCHLA & ASSOCIATES		
DECIMAL ±	200 series	SCALE —	DRAWN BY D / APPROVED BY
FRACTIONAL ±	TITLE SCH: MODEL 208 P.S.S. / part 1 complex osc.		
ANGULAR ±	DATE 7-7-73	DRAWING NUMBER B 2080 - 7A	

180k 13.5V batteries (mfg)

DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
7/7		change R25, 29, 40			



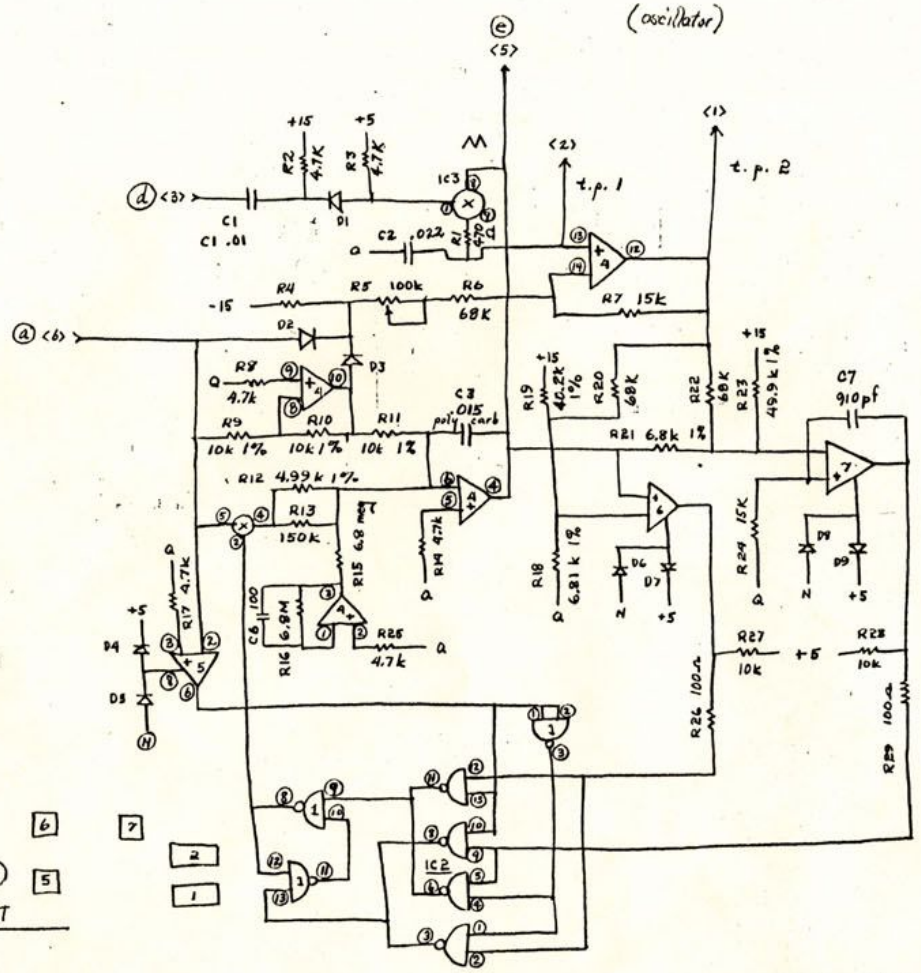
Test: check ∿ @ pin <15>
check sig out @ pin <4>
vary waveshape @ pins <1>, <2>

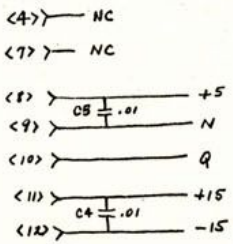
2 trimmers: 1 for low freq linearity off board; 1 for sine wave adj. on board

1 2 3 4
IC layout ①

TOLERANCES (EXCEPT AS NOTED)	BUCHLA & ASSOCIATES		
DECIMAL ±	200 series	SCALE —	DRAWN BY V / APPROVED BY
FRACTIONAL ±	TITLE GCH: MODEL 208 PROG. SOUND SOURCE	part 2 complex osc.	
ANGULAR ±	DATE 7-7-73	DRAWING NUMBER B 2080-8A	

DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.





(consider replacing R5 with fixed R)

4 6 7
3 5 2 1

IC layout

(R7 sets range of feedforward correction for high modulation index. trim with R5)

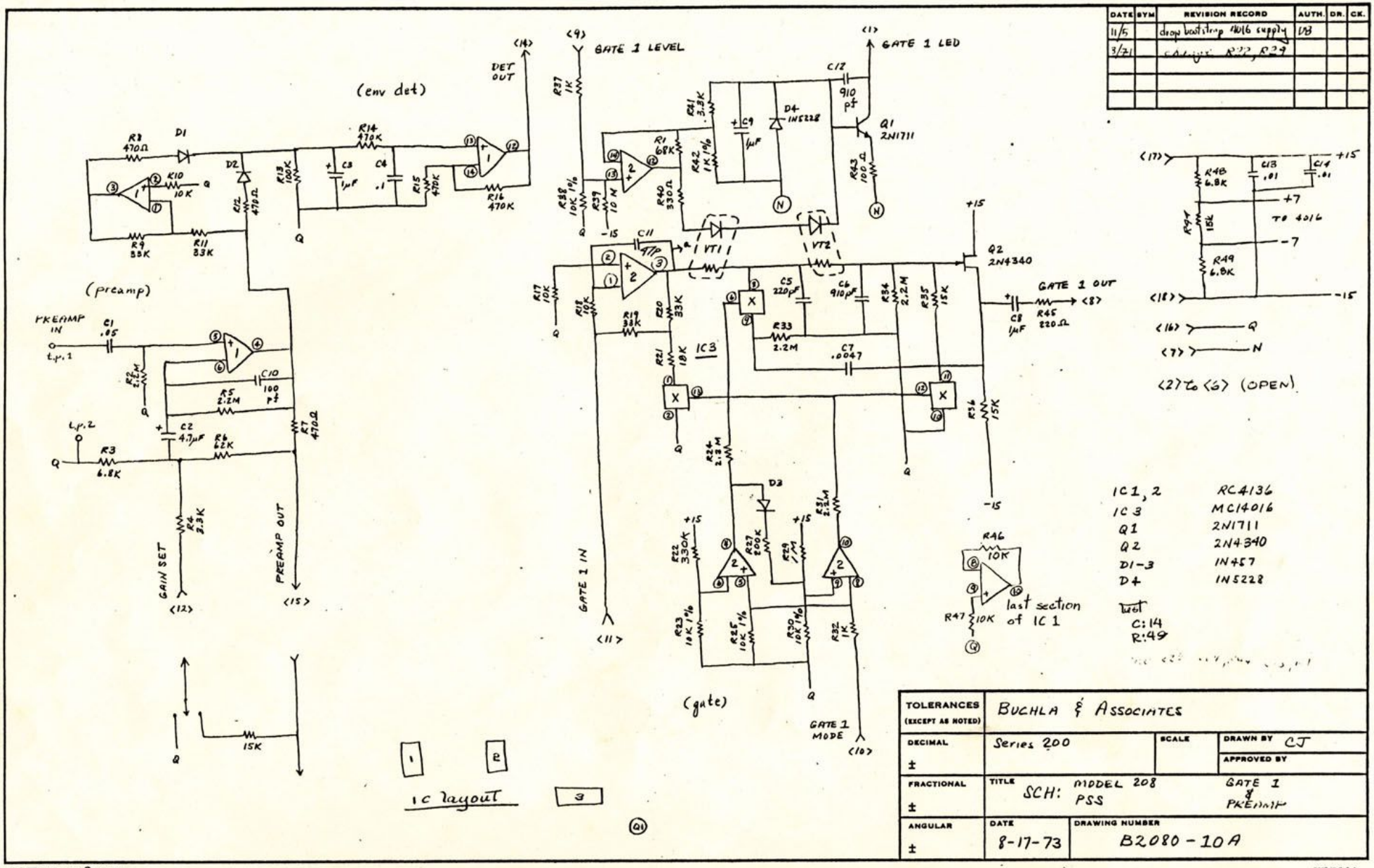
(R's 20, 22 set lock gain (and above))

D1-9	IN457 A
IC 1, 2	MC 846 P
IC 3	DG 200 A
IC 4	RC4136
IC 5-7	301A

last count R30 C7

1 trim on board (tracking adj for high mod. index, vco pitch)

TOLERANCES (EXCEPT AS NOTED)	BUCHLA & ASSOCIATES		
DECIMAL ±	200 series	SCALE —	DRAWN BY D / APPROVED BY
FRACTIONAL ±	TITLE SCH: COMPLEX OSC. PART 3 / PART OF MODEL 208 P.S.S.		
ANGULAR ±	DATE 7-7-73	DRAWING NUMBER B 2080 - 9	



DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
11/5		drop bootstrap 4016 supply	DB		
3/21		change R22, R24			

IC 1, 2	RC4136		
IC 3	MC14016		
Q1	2N1711		
Q2	2N4340		
D1-3	IN457		
D4	IN5228		

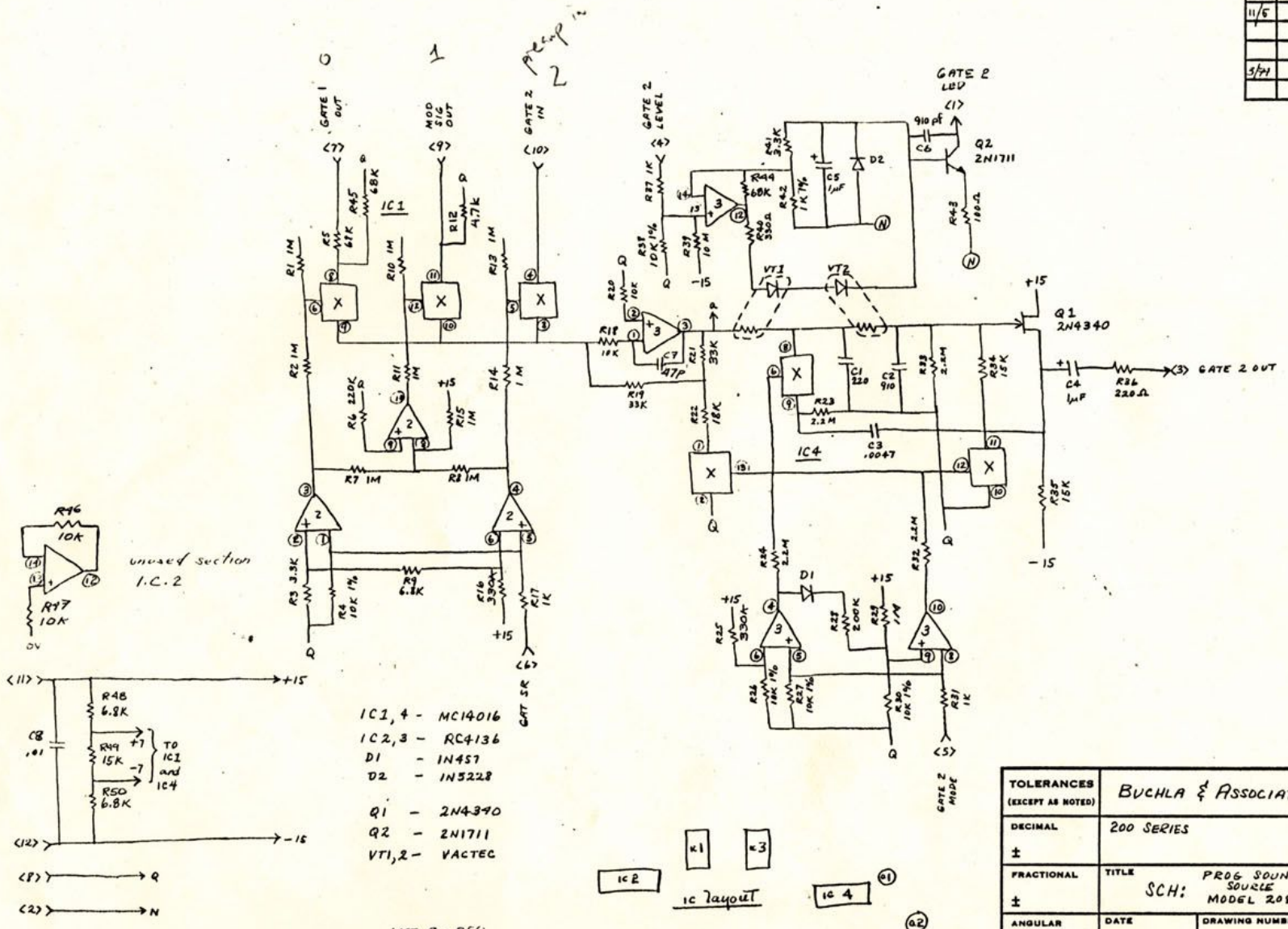
Test
C: 14
R: 49

<2> to <5> (OPEN)

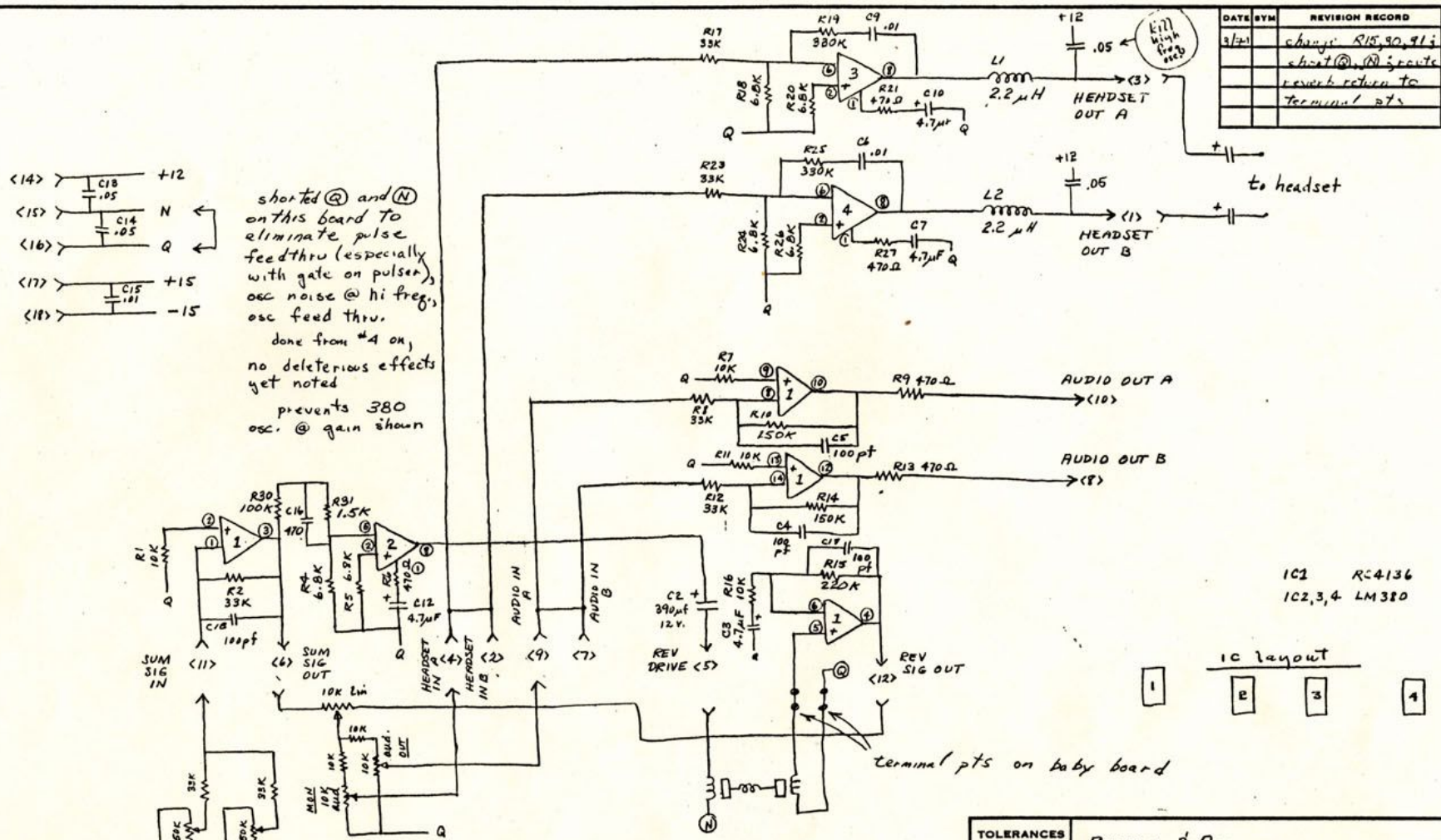
TOLERANCES (EXCEPT AS NOTED)	BUCHLA & ASSOCIATES		
DECIMAL ±	Series 200	SCALE	DRAWN BY CJ; APPROVED BY
FRACTIONAL ±	TITLE SCH: MODEL 208 PSS		GATE 1 & PREAMP
ANGULAR ±	DATE 8-17-73	DRAWING NUMBER B2080-10A	

10

DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
11/6		drop bootstrapped supply			
		To IC4			
		change pin 9 tieoff around			
5/74		change R16, R25, R29			

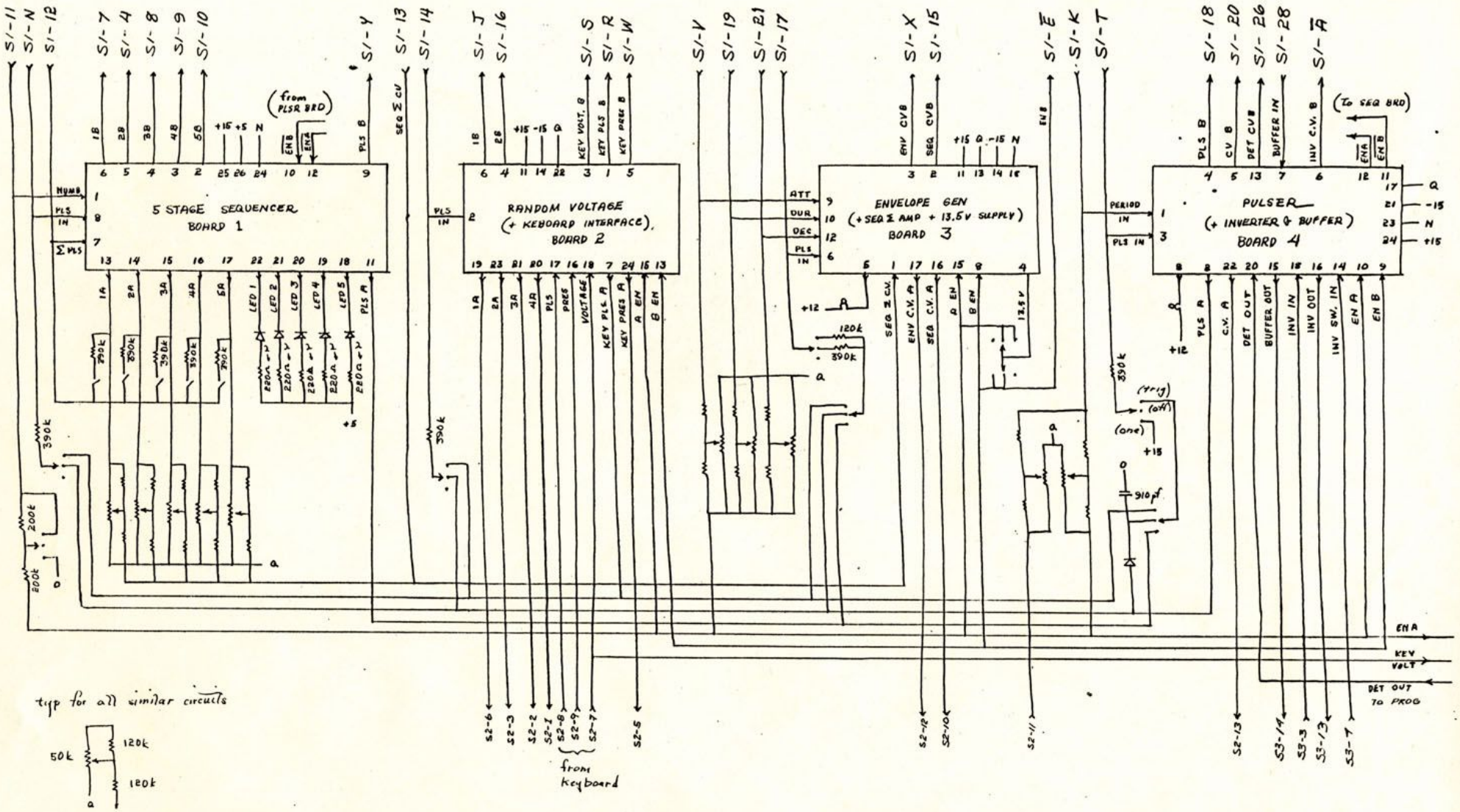


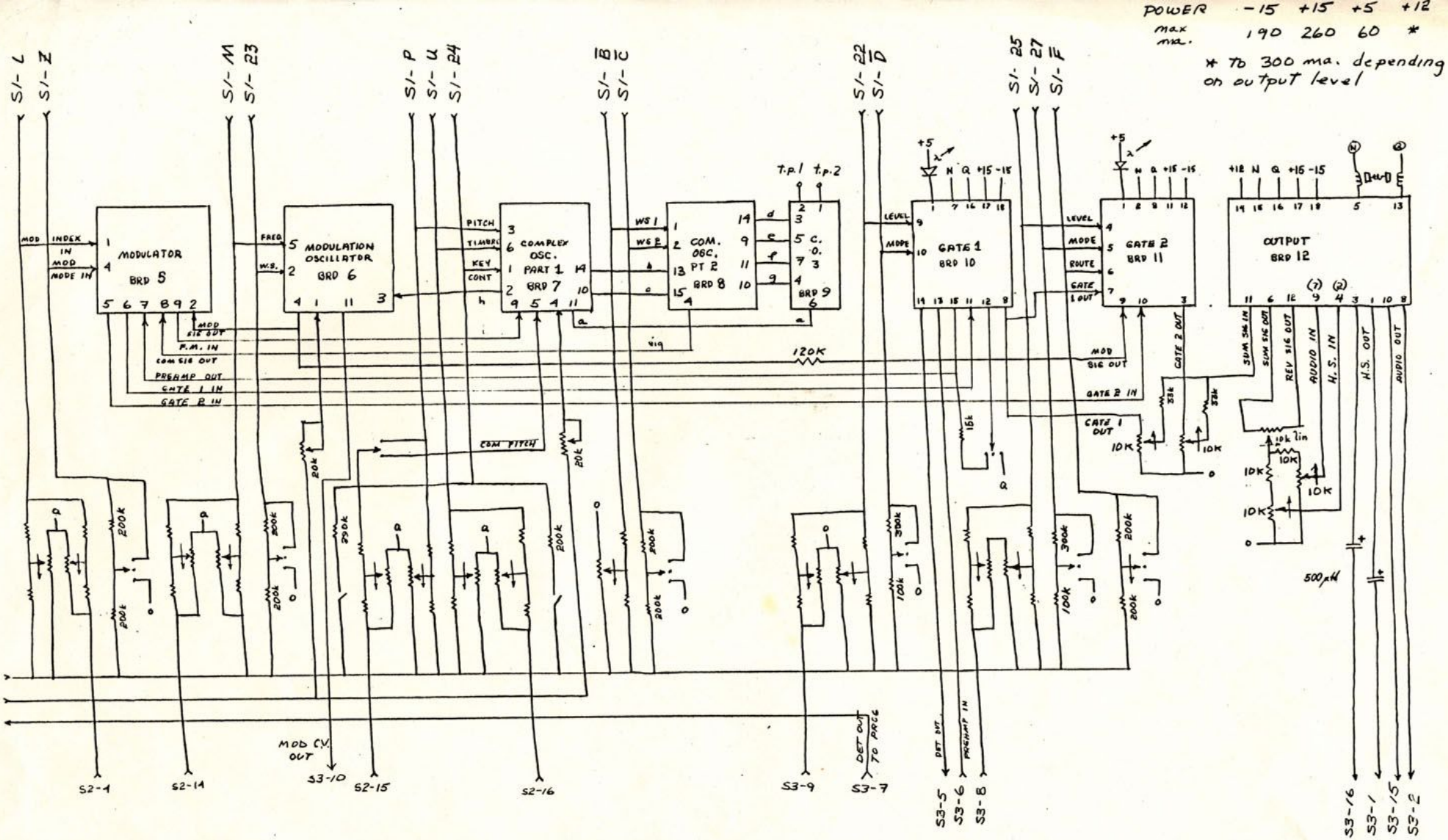
TOLERANCES (EXCEPT AS NOTED)	BUCHLA & ASSOCIATES		
DECIMAL ±	200 SERIES	SCALE	DRAWN BY CJ / APPROVED BY
FRACTIONAL ±	TITLE SCH: PROG SOUND SOURCE MODEL 208		GATE 2
ANGULAR ±	DATE 8-10-73	DRAWING NUMBER B2080-11A	



DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
9/71		change R15, 90, 91; short Q, N; route reverb return to terminal pts			

TOLERANCES (EXCEPT AS NOTED)	BUCHLA & ASSOCIATES		
DECIMAL ±	200 Series	SCALE	DRAWN BY CJ; APPROVED BY
FRACTIONAL ±	TITLE SCH: MODEL 208 PSS OUTPUT		
ANGULAR ±	DATE 8-17-73	DRAWING NUMBER B2080-12A	


5 STAGE SEQUENCER BOARD 1
RANDOM VOLTAGE (+ KEYBOARD INTERFACE), BOARD 2
ENVELOPE GEN (+ SEQ Σ AMP + 13.5V SUPPLY) BOARD 3
PULSER (+ INVERTER & BUFFER) BOARD 4
(from PLSR BRD)
(To SEQ BRD)
tap for all similar circuits
50k
120k
120k
BUCHLA ASSOC.
B2080-13


POWER -15 +15 +5 +12
max ma. 190 260 60 *
* To 300 ma. depending on output level
MODULATOR BRD 5
MODULATION OSCILLATOR BRD 6
COMPLEX OSC. PART 1 BRD 7
COM. OSC. PT 2 BRD 8
BRD 9
GATE 1 BRD 10
GATE 2 BRD 11
OUTPUT BRD 12
120K
MOD CV OUT
COM PITCH
DET OUT TO PROG
DET OUT
PREAMP IN
S2-1
S2-14
S3-10
S2-15
S2-16
S3-9
S3-7
S3-5
S3-6
S3-8
S3-16
S3-1
S3-15
S3-2
BUCHLA ASSOC
B2080-14