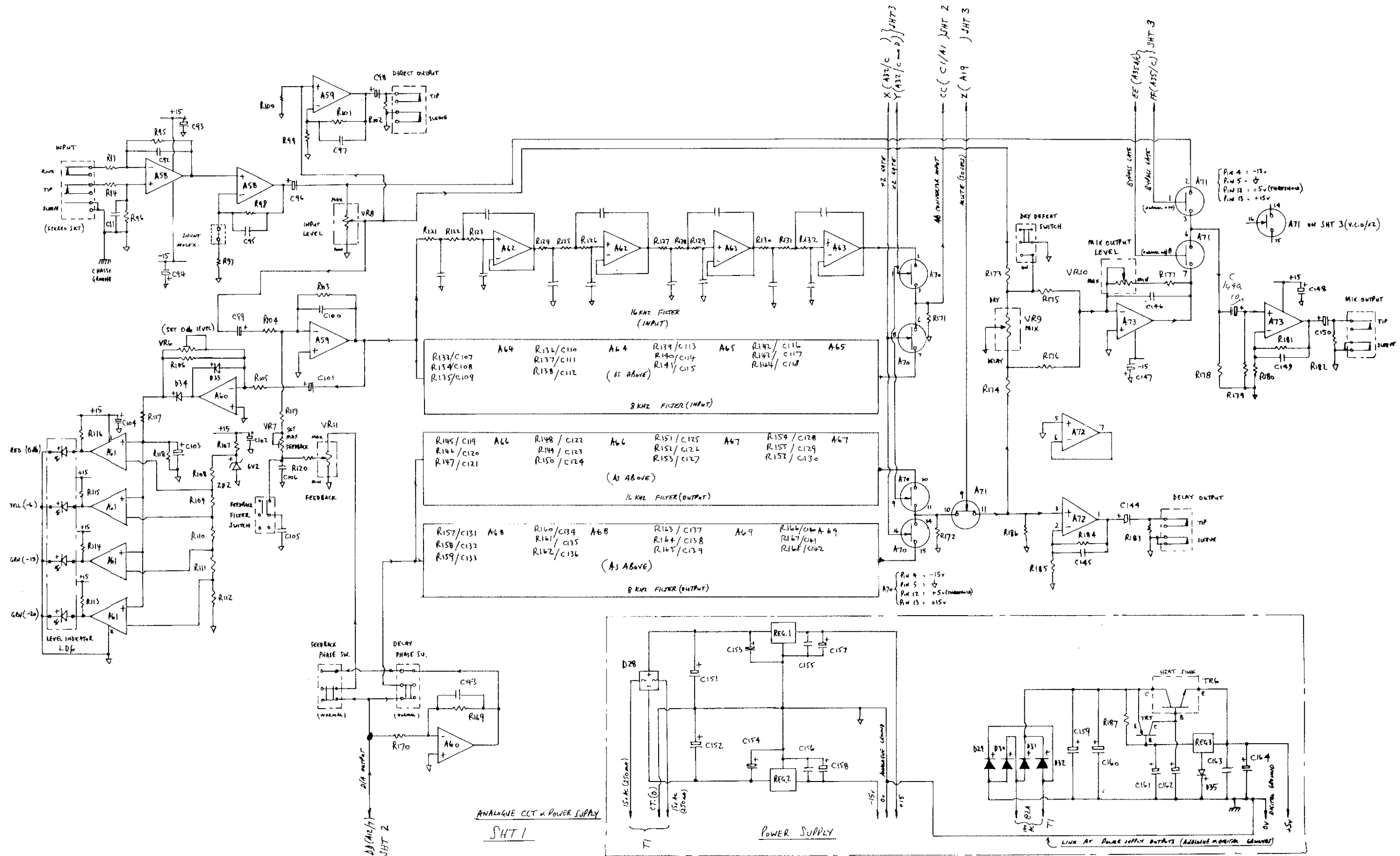
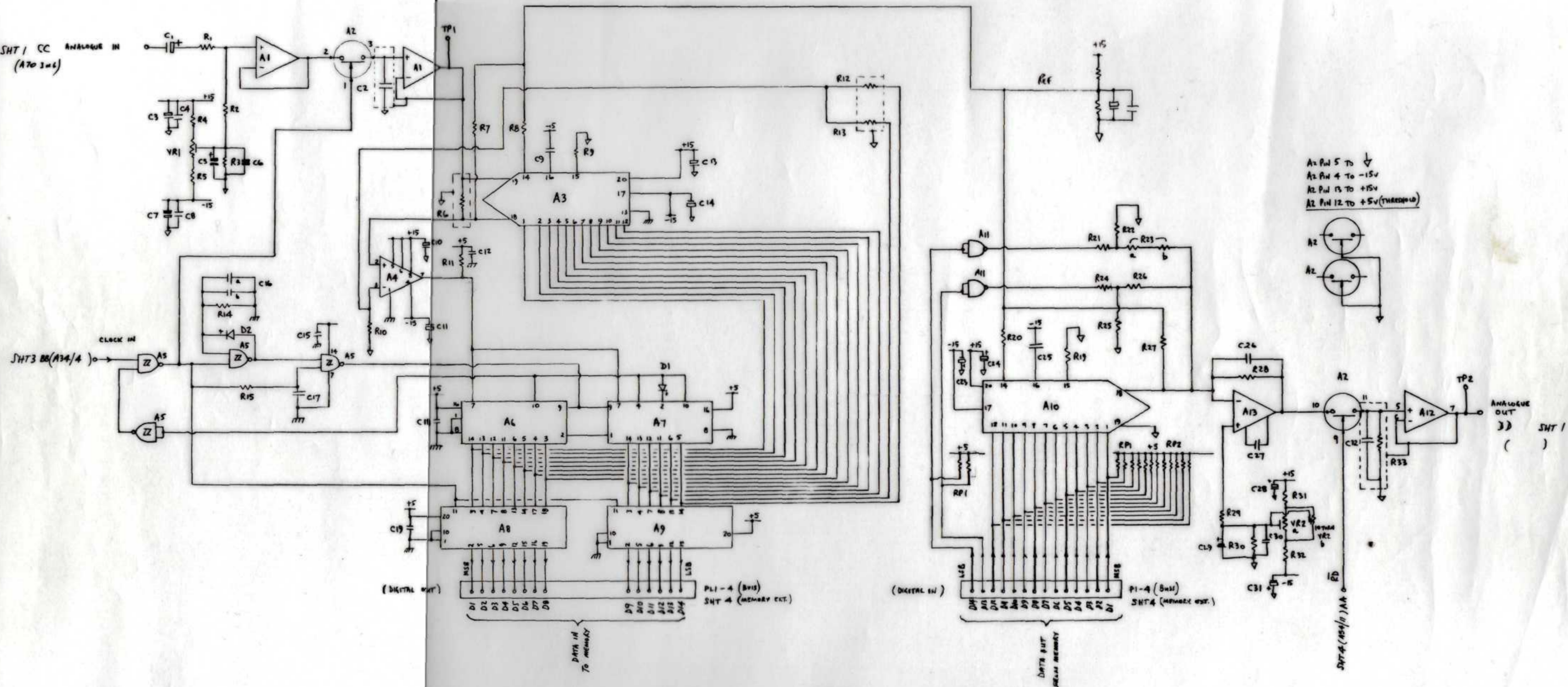
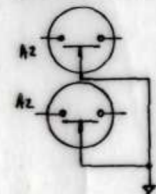




SHT 1 CC ANALOGUE IN
(A70 3u6)

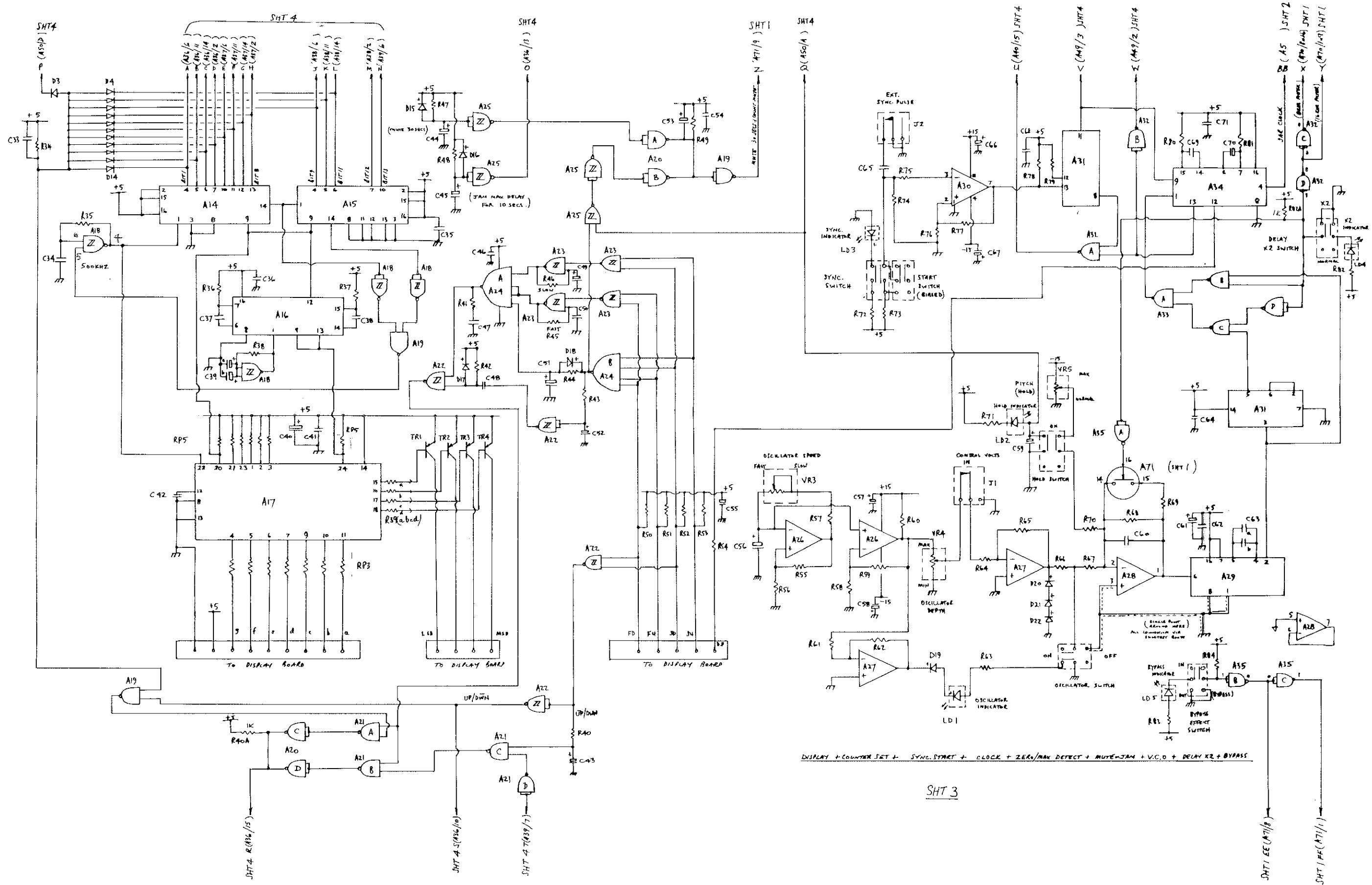


A2 Pin 5 To $\downarrow$
 A2 Pin 4 To -15V
 A2 Pin 15 To +15V
 A2 Pin 12 To +5V (THRESHOLD)



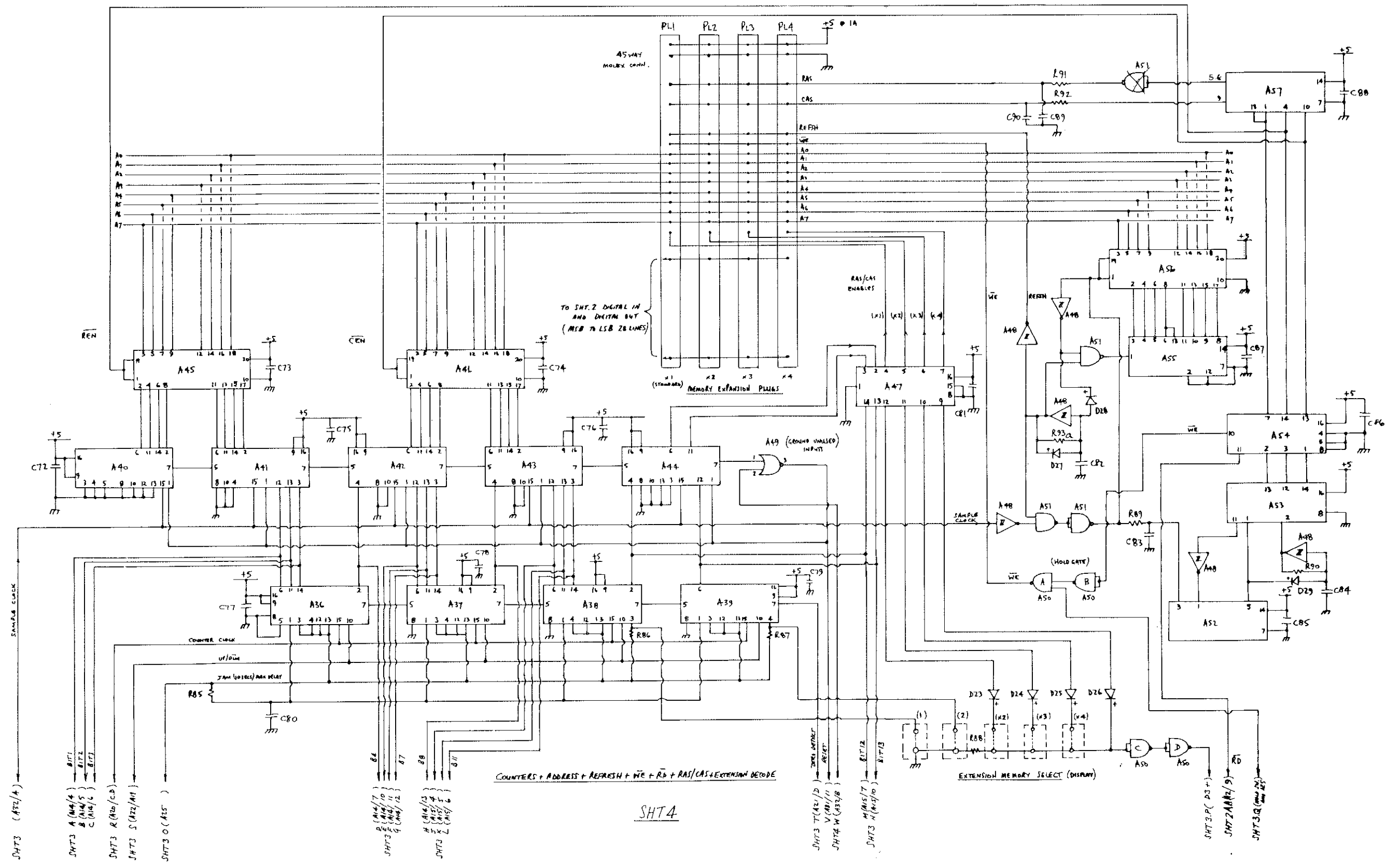
SHT 2

ANALOGUE TO DIGITAL AND DIGITAL TO ANALOGUE CONVERSION

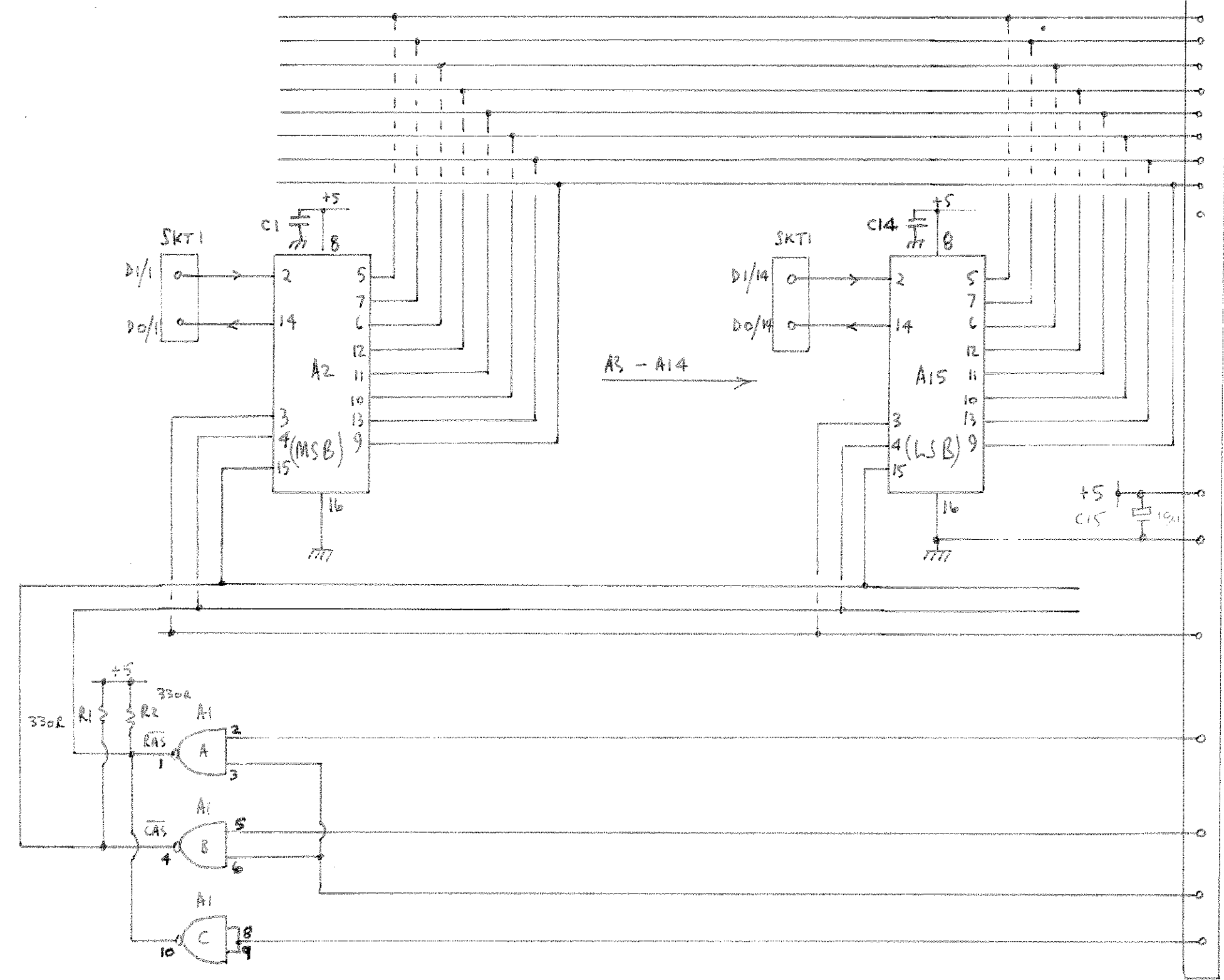


DISPLAY + COUNTER SET + SYNC START + CLOCK + ZERO/MAX DETECT + MUTE-JAN + V.C.O + DELAY X2 + BYPASS

SHT 3



SKT1 (45 WAY MOLEX)



NOTE
256K DRAM
1 EXTRA ADDRESS NEEDED
A8 CONNECTED TO DRAM PIN 1

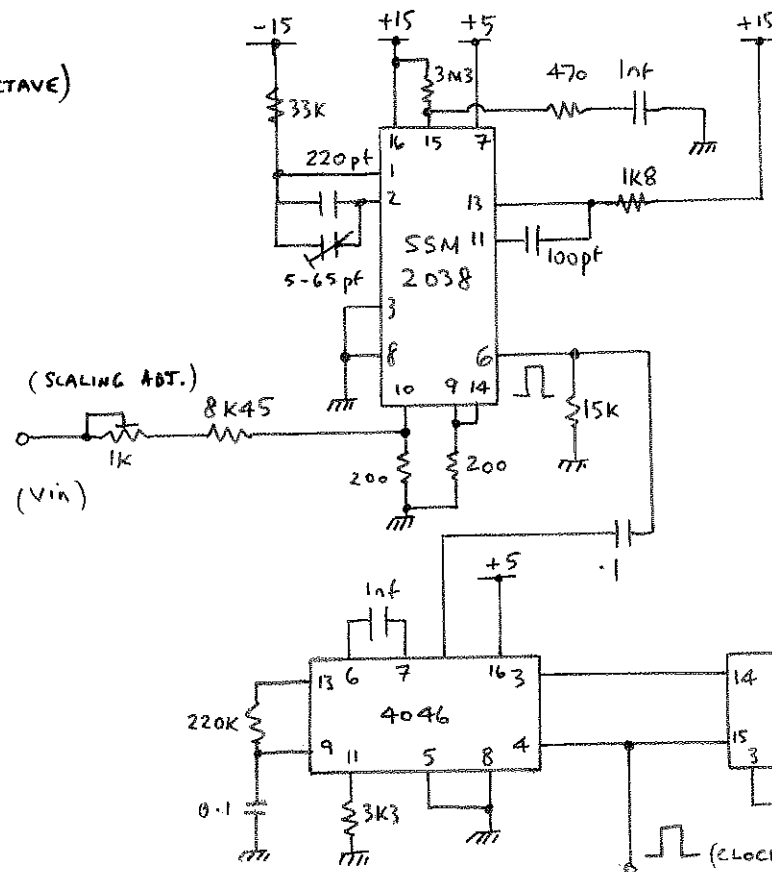
+5V
GROUND

WE
RAS
CAS
RAS x CAS ENABLE
REFRESH

ISSUE	DESCRIPTION	APPD.	DATE	TITLE	DRAWN	TRACED	CHECKED	APPROVED	DATE
				DRAM MEMORY BOARD.					
				(64K)					

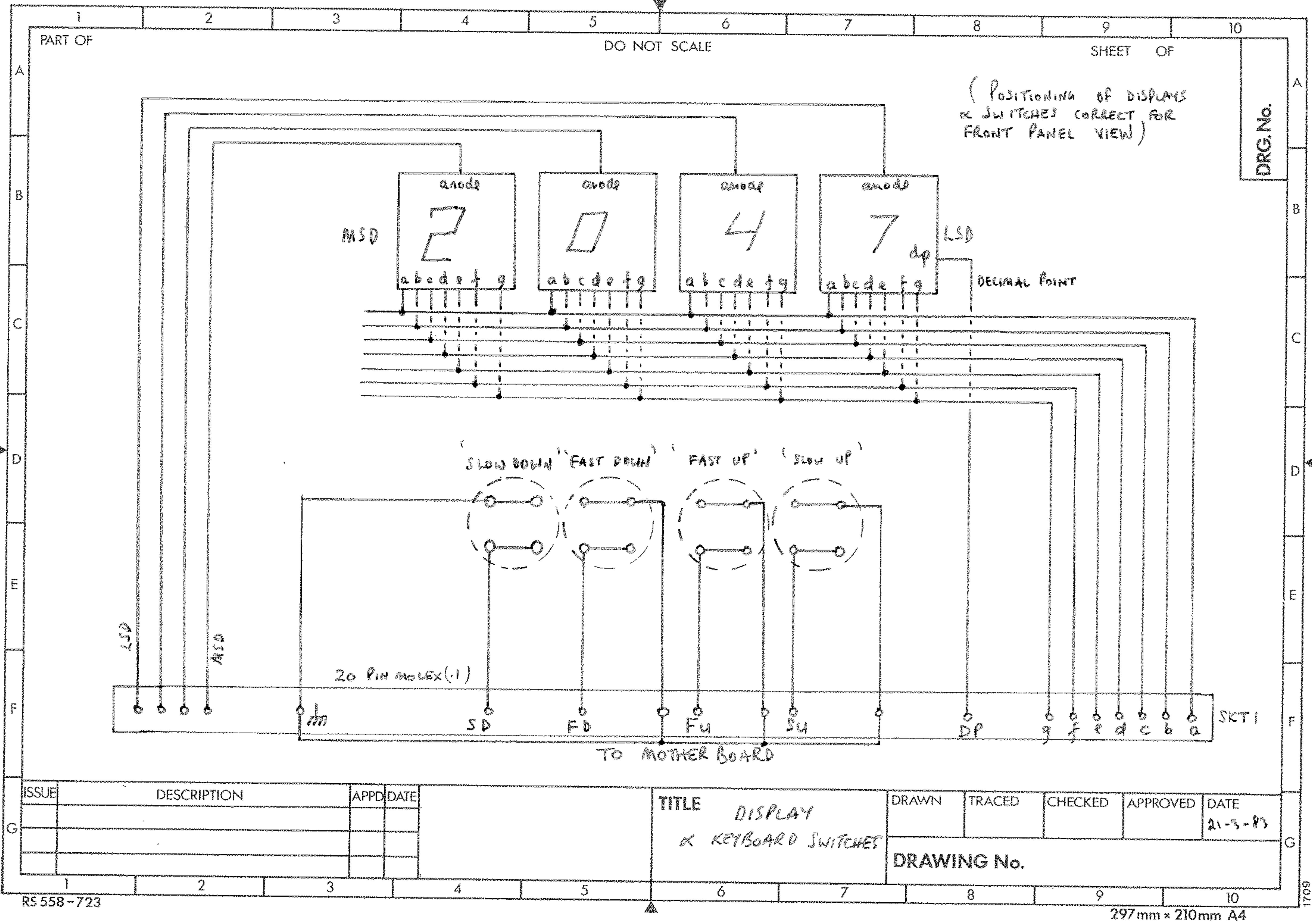
BEL B080

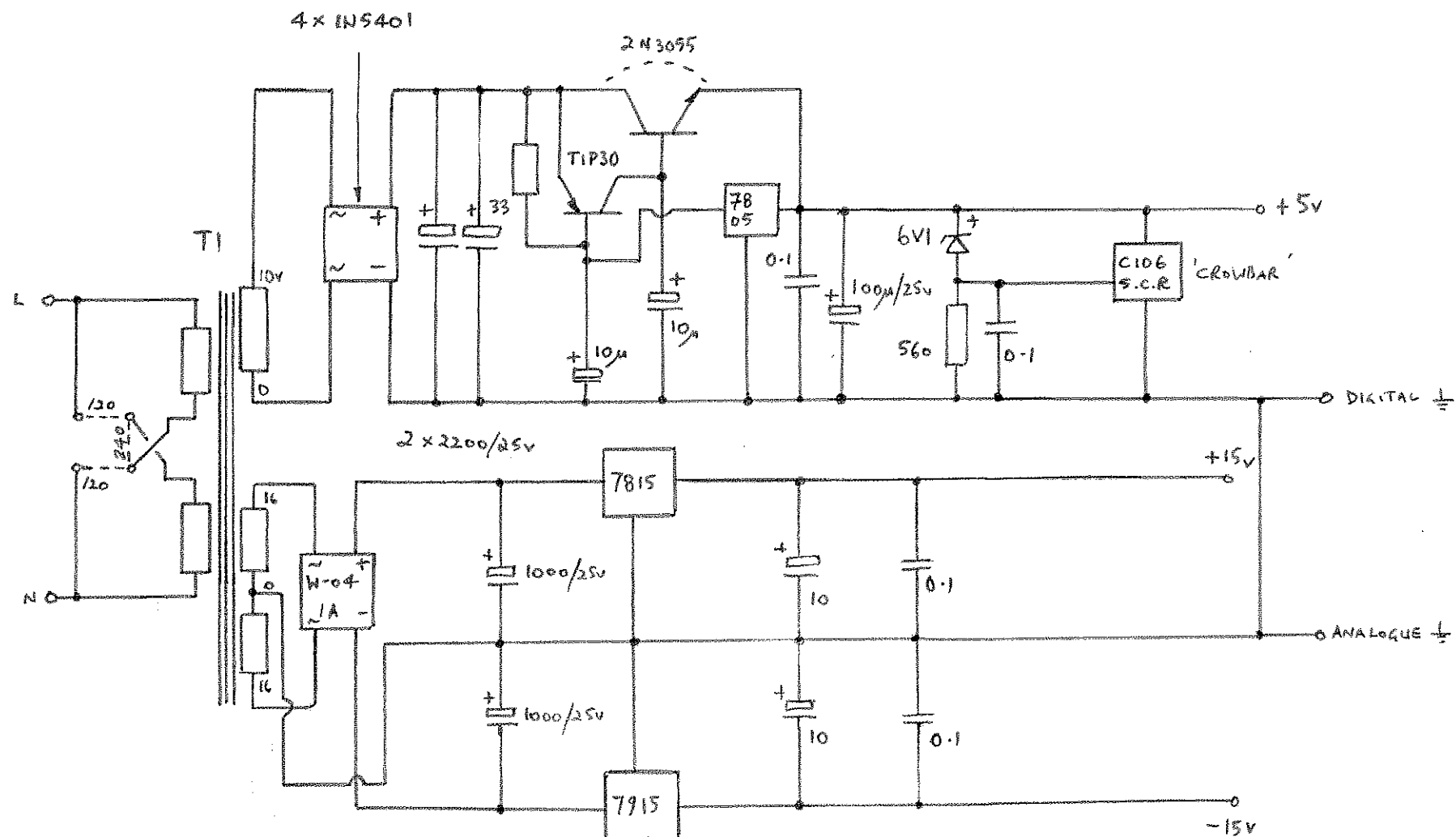
CLOCK CIRCUIT (1V/OCTAVE)



10 WAY MOLEX.

- PIN 4 = CLOCK OUT
- PIN 5 = +5V
- PIN 6 = +15V
- PIN 7 = pin
- PIN 8 = -15V
- PIN 9 = +5V
- PIN 10 = Vin





ISSUE	DESCRIPTION	APPD	DATE

1. **Introduction**
 2. **Background**
 3. **Methodology**
 4. **Results**
 5. **Conclusion**

BD80
POWER SUPPLY

DRAWN

DA 9/2/84

TRACED

CHECKED

APPROVED

DATE

10-2-84

DRAWING No.