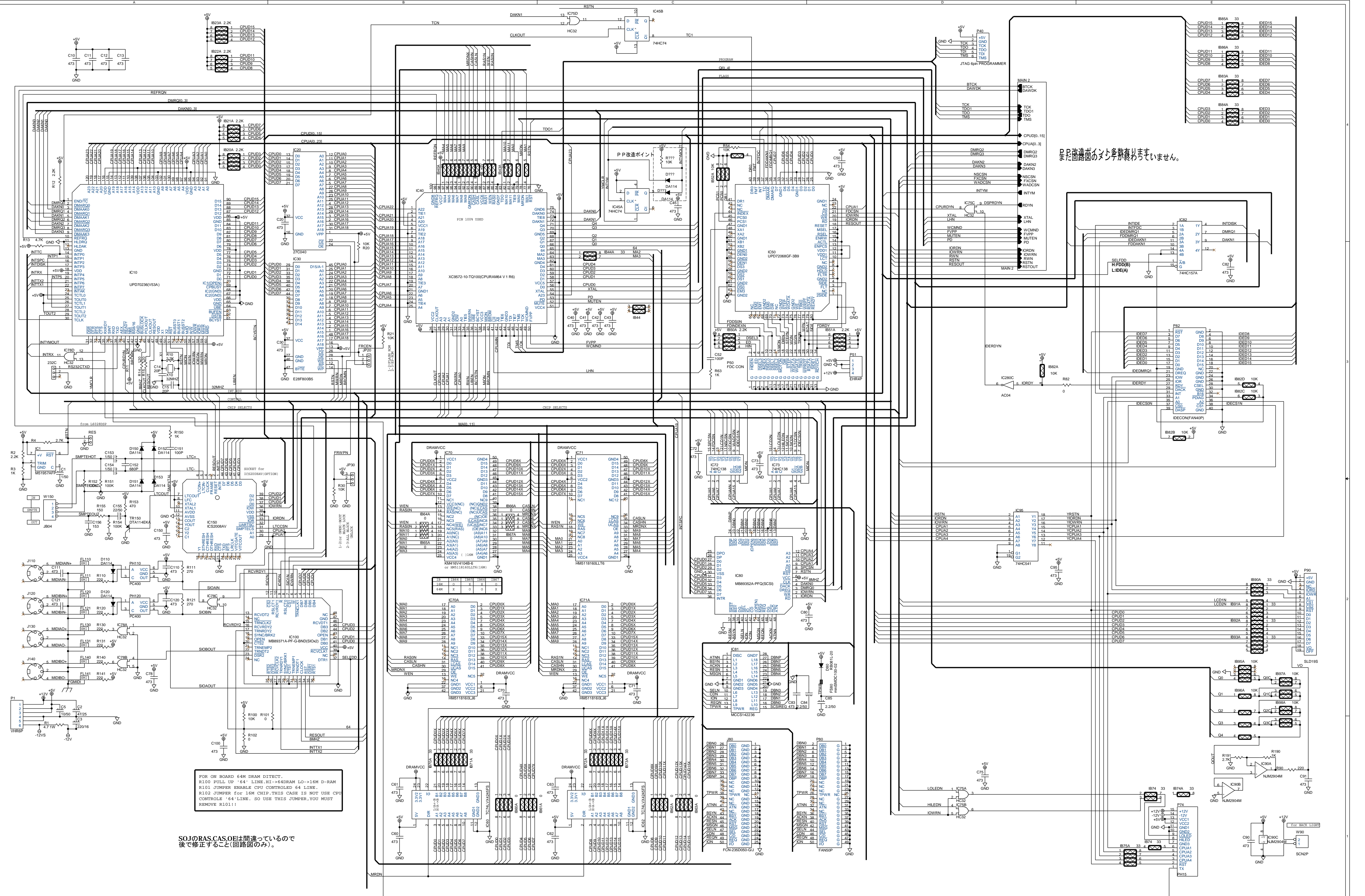


C 424は3ピンと4ピンの近くに配置すること。

REVISION		1st EDITION		DESIGNED		APPROVED		CHECKED	
---	---	---	---	---	---	---	---	---	---
---	---	---	---	---	---	---	---	---	---
---	---	---	---	---	---	---	---	---	---
---	---	---	---	---	---	---	---	---	---
---	---	---	---	---	---	---	---	---	---
---	---	---	---	---	---	---	---	---	---
---	---	---	---	---	---	---	---	---	---

CIRCUIT NO.		L6044801	
Design File:	C:\WORK\IIPC2000X\L\q.b.c\win\TH\IIPC2000X\MAIN 3/3 (ANALOG)	Rev	1
Design Name:	MAIN 3/3 (ANALOG)	Rev	1
Schematic Name:	ANALOG	Size	0.5
Description:	(Doc)	Size	A2
Created:	Monday, July 13, 1998	Created:	Monday, July 13, 1998
Modified:	Tuesday, January 05, 1999	Modified:	Tuesday, January 05, 1999
AKAI ELECTRIC CO.,LTD.		AKAI ELECTRIC CO.,LTD.	



FOR ON BOARD 64M DRAM DETECT.
R100 PULL UP '64' LINE. HI->64DRAM LO->16M-D-RAM
R101 JUMPER ENABLE CPU CONTROLLED 64 LINE.
R102 JUMPER FOR 16M CHIP. THIS CASE IS NOT USE CPU
CONTROLLE '64'LINE. SO USE THIS JUMPER, YOU MUST
REMOVE R101!!

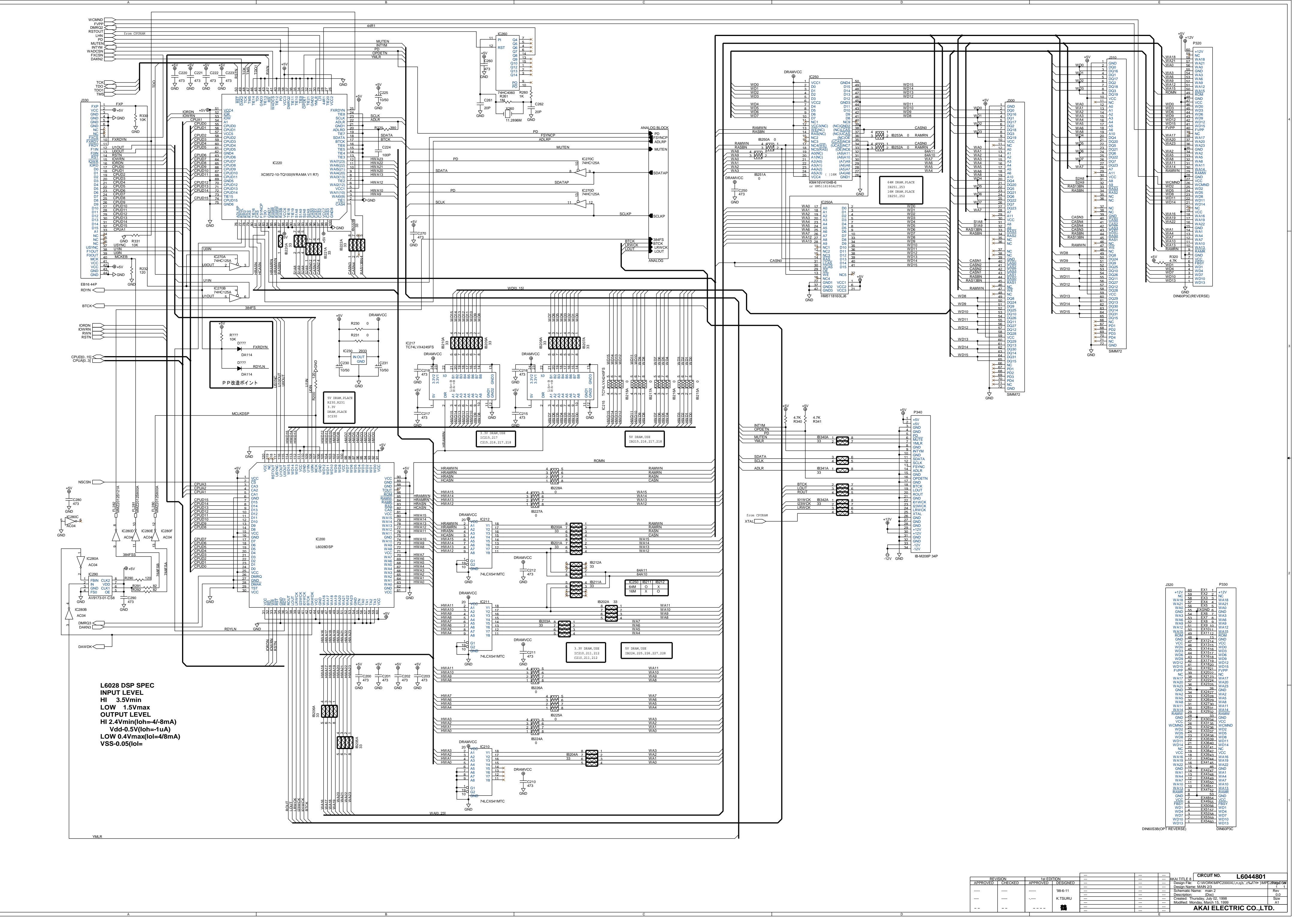
SOJのRAS,CAS,OEは間違っているので
後で修正すること(回路図のみ)。

CASE FOR 3.3V DRAM, PLACE
IC60, 61, 62, 63
CASE FOR 5V DRAM, PLACE
IB60, 61, 62, 63

まだ回路図の修正が完了していません。

REV/ISSN	CHECKED	APPROVED	DESIGNED	DATE	DESIGNER	CIRCUIT NO.
1.0				199-7-9		L6044801
1.0				199-8-11	K.TSURU	

AKAI TITLE 8
Design File: C:\WORK\MPC2000\LDG_276\FM_TAMP_Rap001.cdr
Design Name: (Em)
Schema Name: main 1
Created: Tuesday, July 07, 1998
Modified: Monday, July 14, 1998
Size
Sheet
Page 11 of 11
AKAI ELECTRIC CO.,LTD.



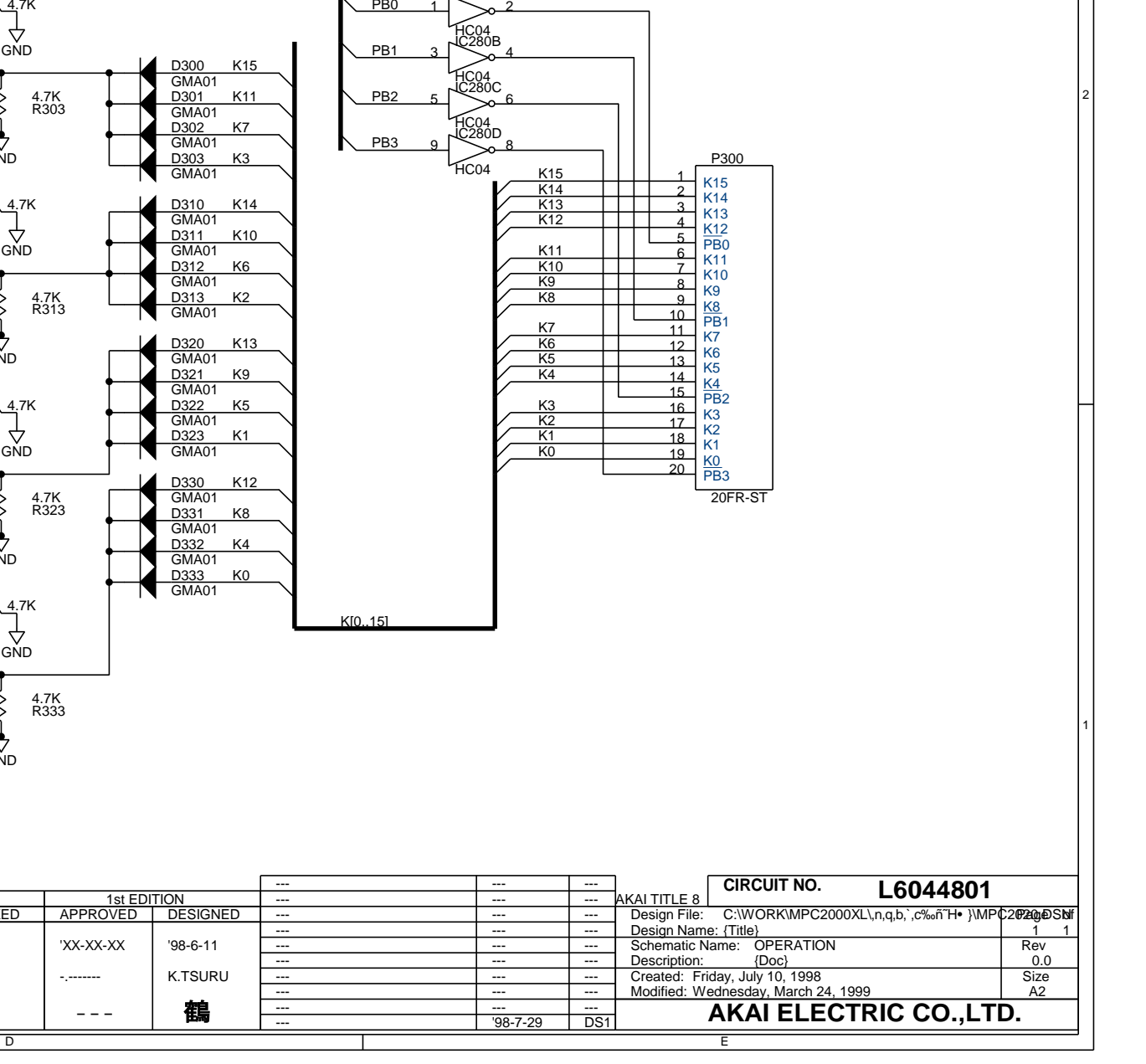
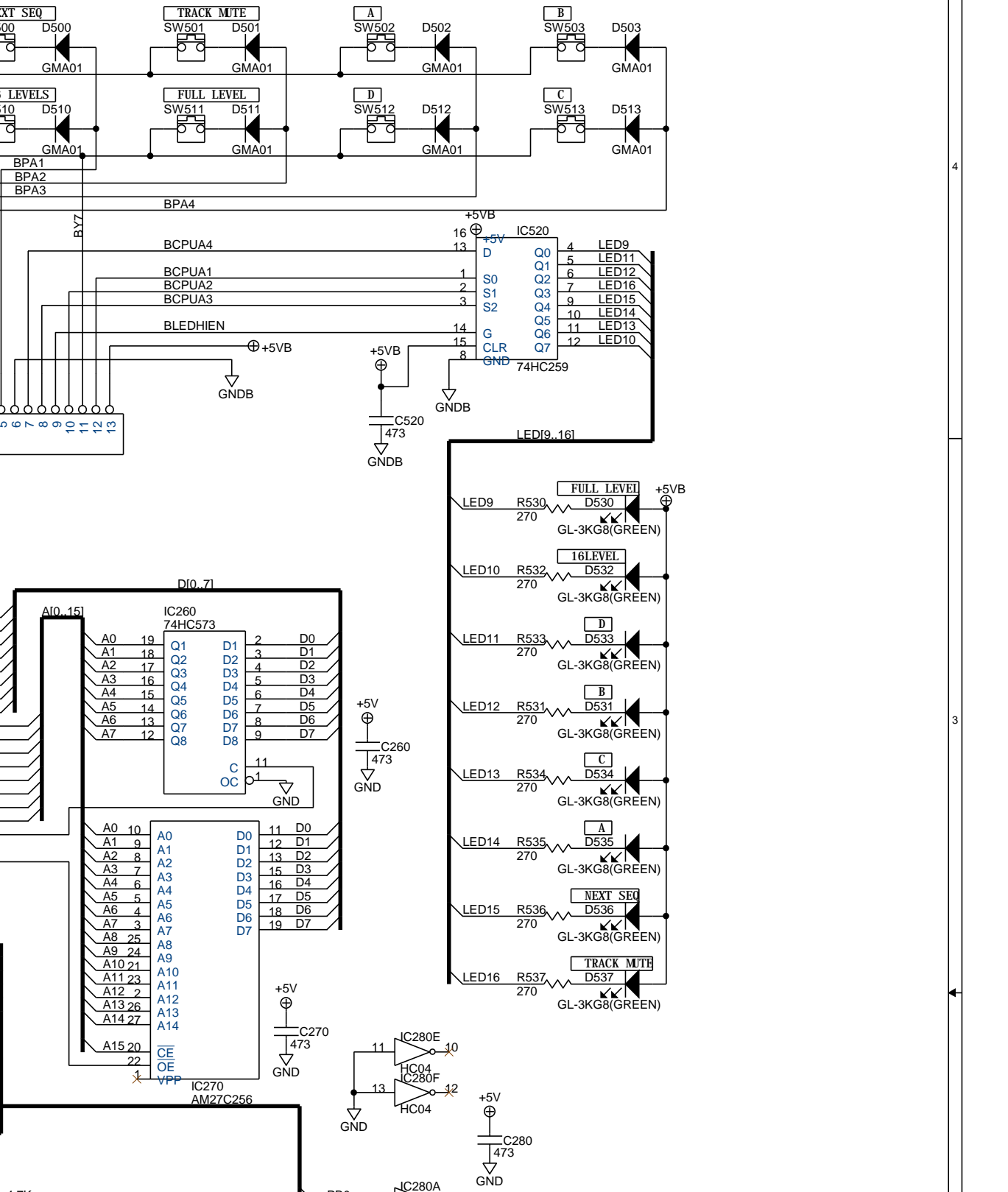
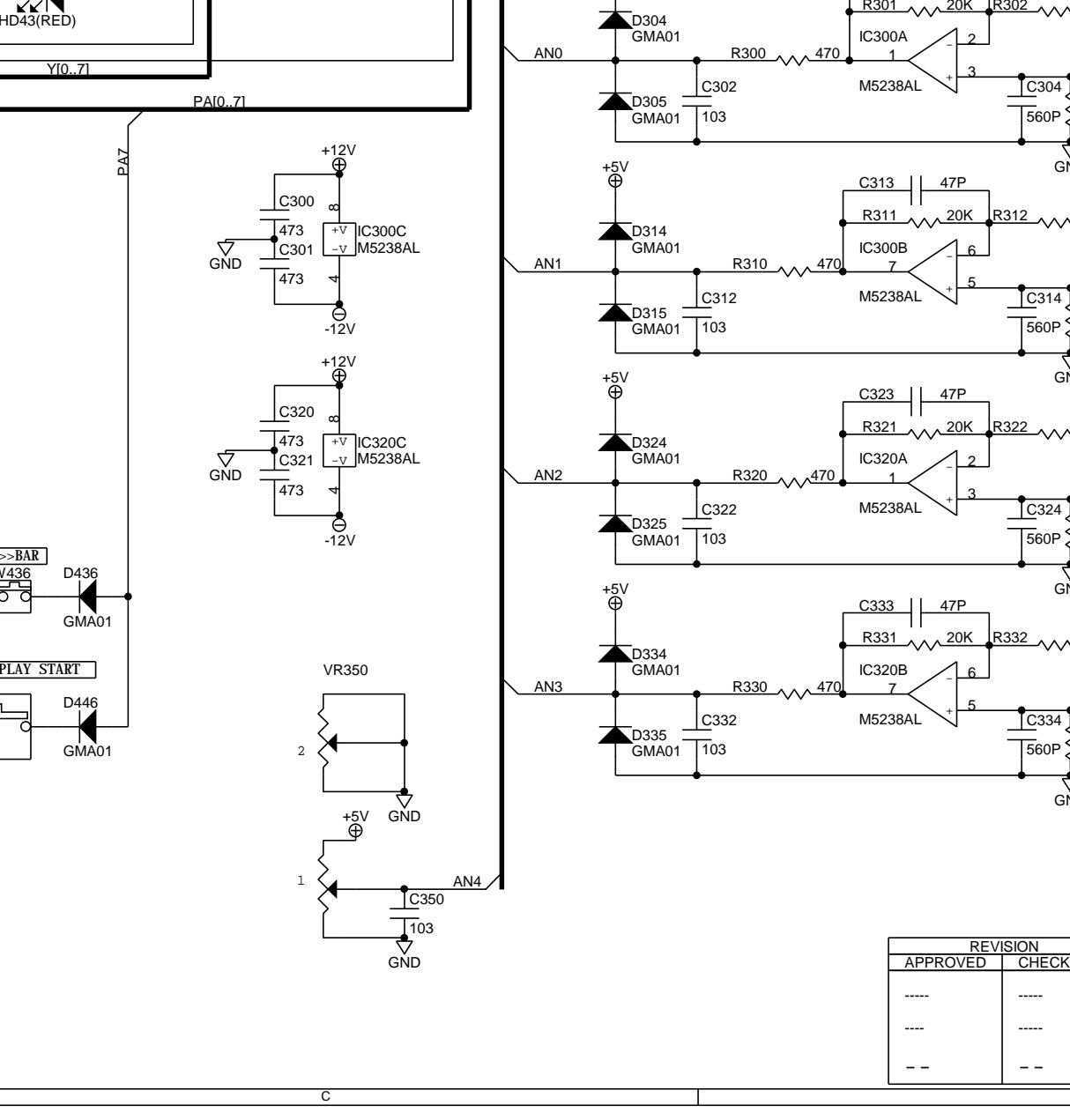
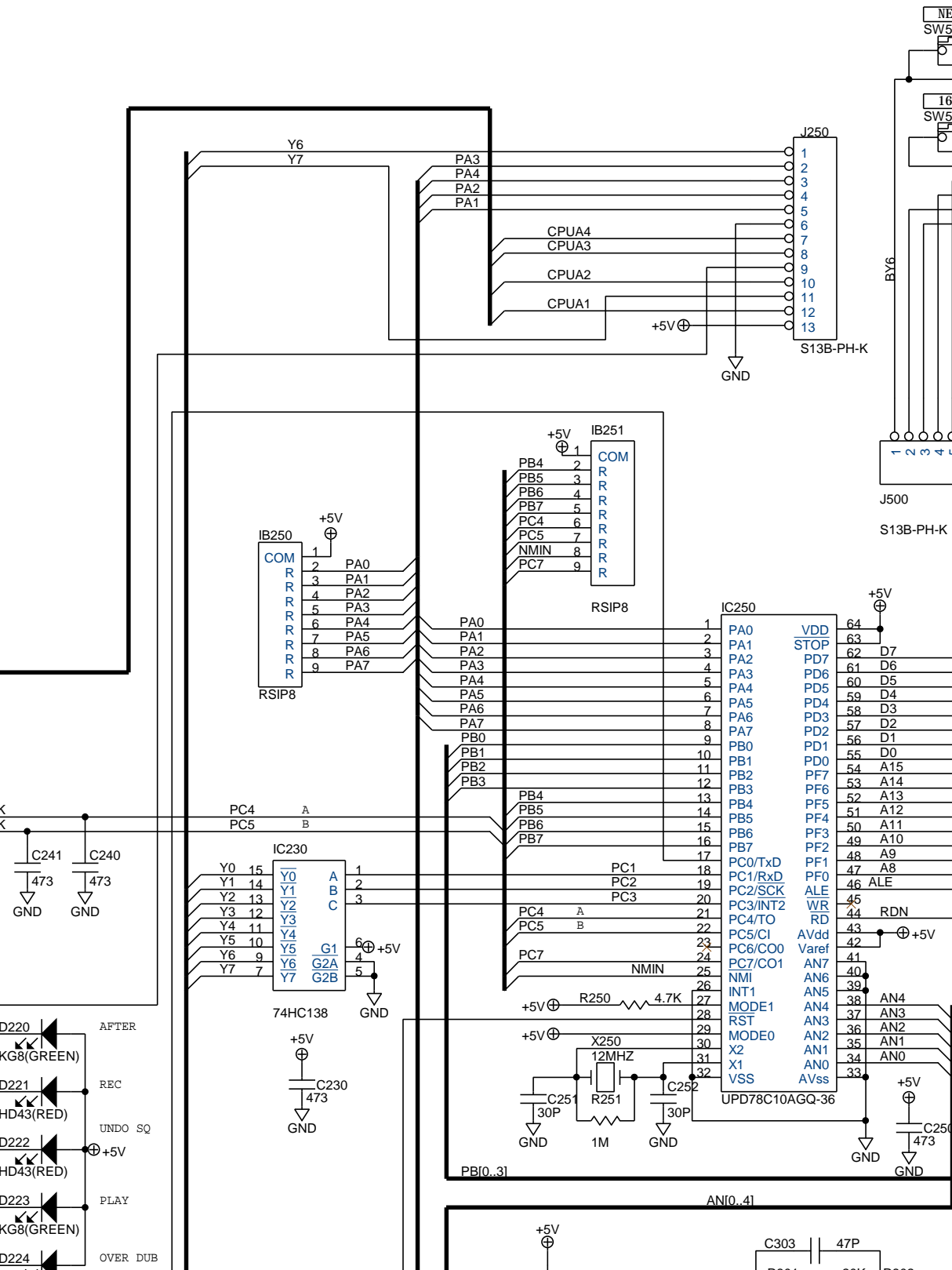
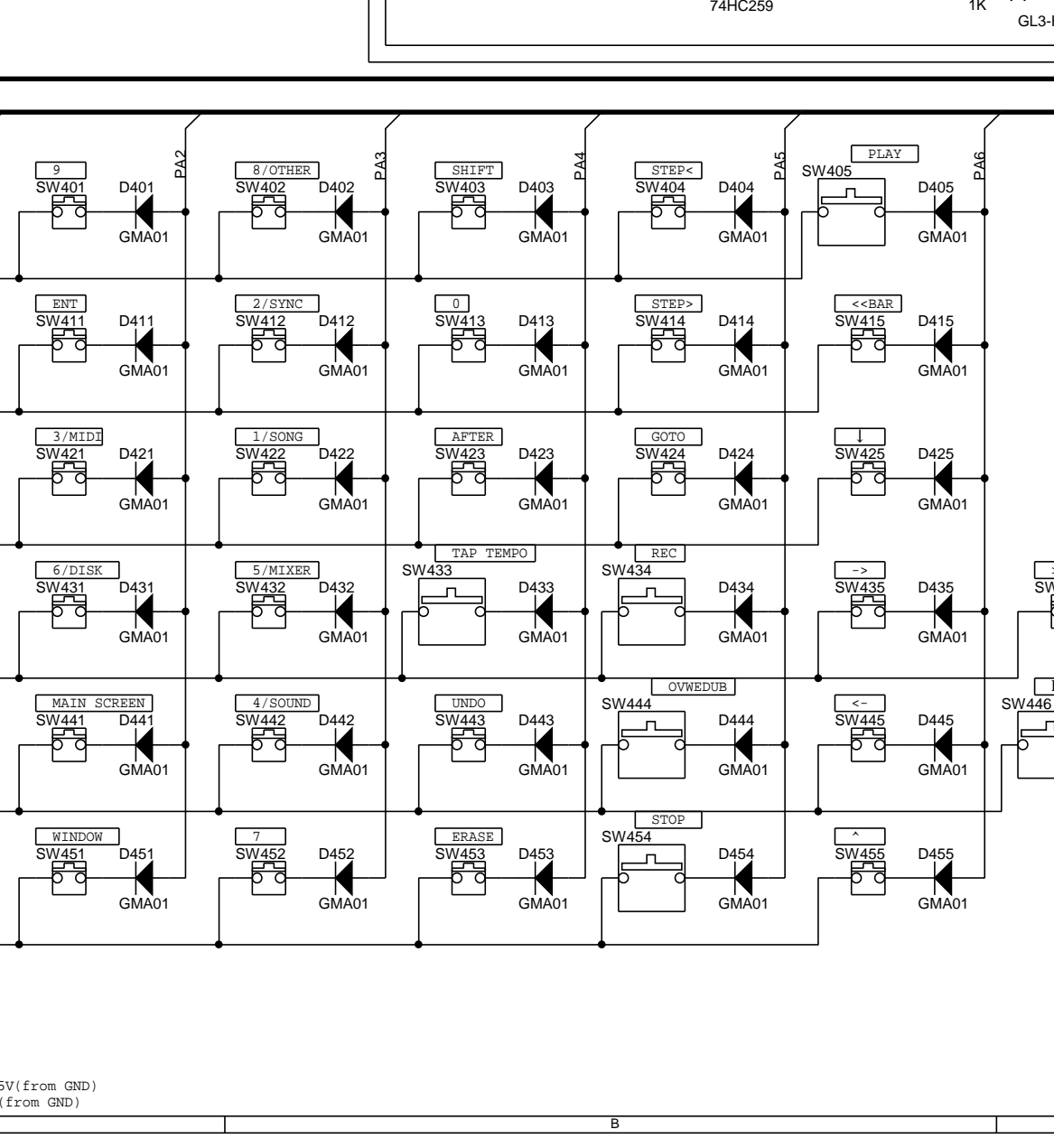
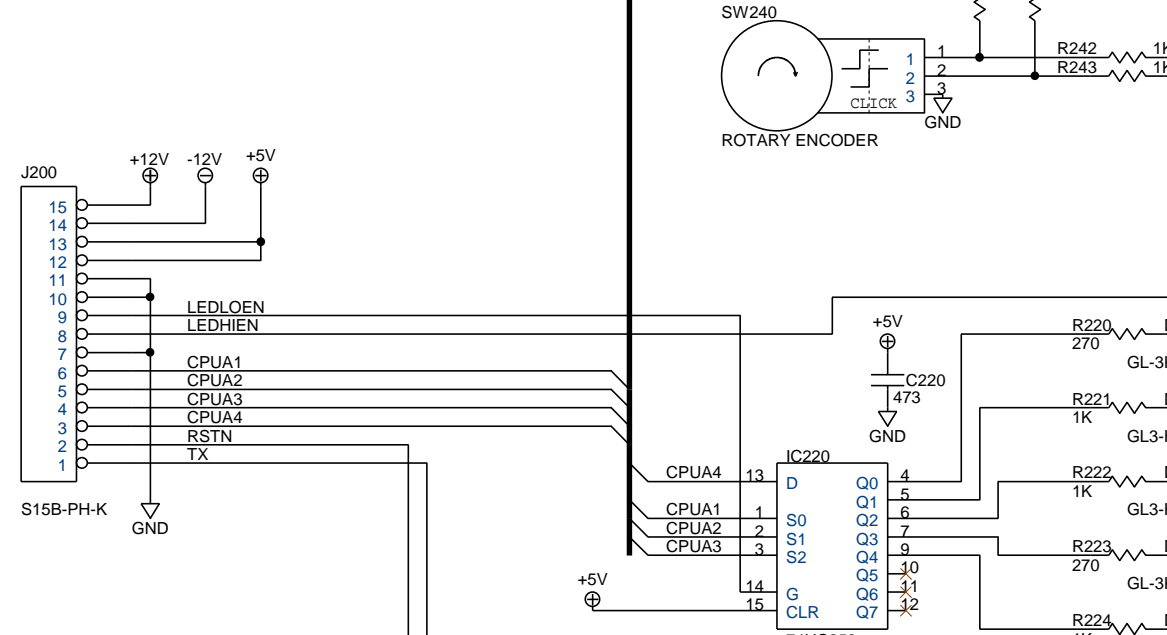
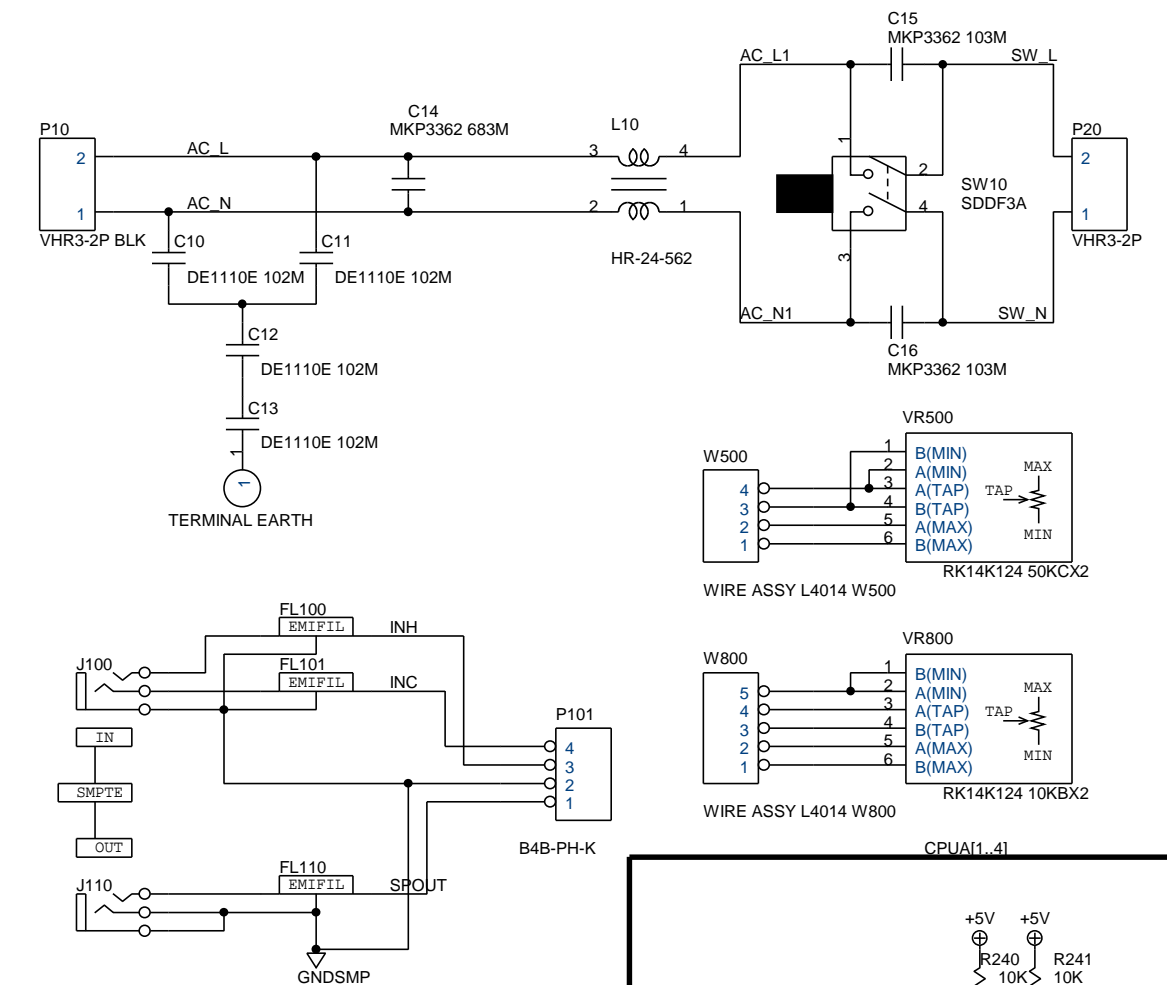
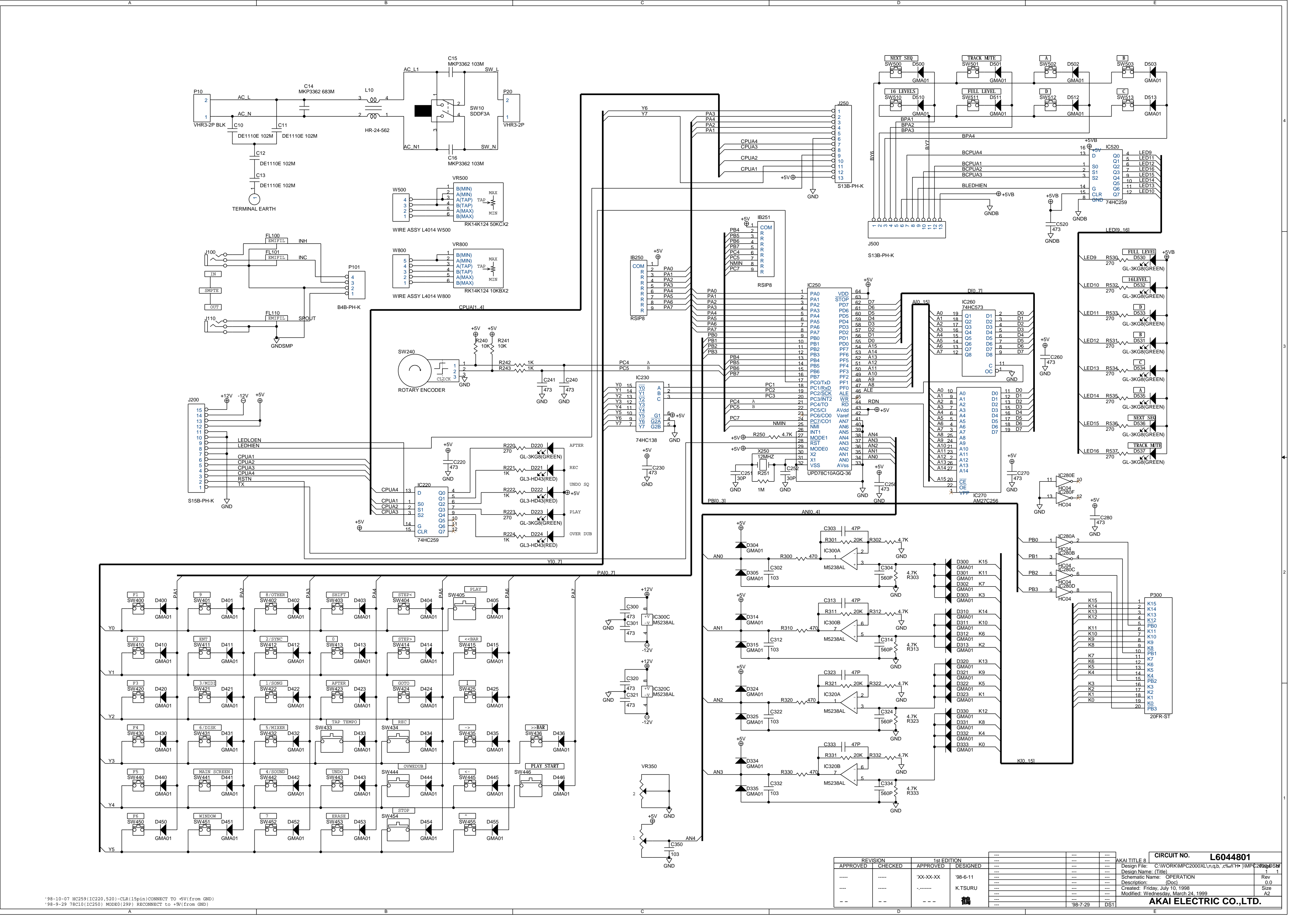
L6028 DSP SPEC
INPUT LEVEL
 HI 3.5Vmin
 LOW 1.5Vmax
OUTPUT LEVEL
 HI 2.4Vmin(IoH=4/8mA)
 Vdd=0.5V(IoH=1uA)
 LOW 0.4Vmax(IoL=4/8mA)
 VSS=0.05(IoL=)

REV	DESCRIPTION	DATE	BY	CHK
1	INITIAL	1998.07.02	K.TSURU	
2	REVISED	1998.07.02	K.TSURU	

REV	DESCRIPTION	DATE	BY	CHK
1	INITIAL	1998.07.02	K.TSURU	
2	REVISED	1998.07.02	K.TSURU	

AKAI TITLE 8
 CIRCUIT NO. L6044801
 Design File: C:\WORK\MPC2000\LAB_250\PP_TAMP_C9903901
 Design Name: Main_2
 Schematic Name: main_2
 Created: Thursday, July 02, 1998
 Modified: Monday, March 16, 1999
 Size: 10.0
 Rev: 0.0

AKAI ELECTRIC CO.,LTD.



*98-10-07 IC250(520)-CLR(15pin)CONNECT TO +5V(from GND)
*98-9-29 78C10(IC250) MODE0(29P) RECONNECT TO +5V(from GND)

Table with 4 columns: REVISION, CHECKED, APPROVED, and 1st EDITION. Includes design file path, title block, and company name AKAI ELECTRIC CO.,LTD.